

YONGJUN PARK

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RESEARCH INTERESTS

My interests include low-power and high performance computer architectures and compilers for mobile devices. I first focus on various compiler solutions that solve inefficiency problem in both VLIW and SIMD accelerators. Moreover, I develop new scalable multicore accelerators for mobile systems, which can efficiently support both instruction and data level parallelism.

EDUCATION

- 09/2007 – Present **University of Michigan, Ann Arbor, MI**
- Ph.D. in Electrical Engineering
- Advised by Prof. Scott Mahlke
- 09/2007 – 04/2009 **University of Michigan, Ann Arbor, MI**
- M.S.E in Electrical Engineering
- GPA: 7.76/9.0
- 03/1999 – 02/2007 **Pohang University of Science and Technology (POSTECH), Pohang, Korea**
- B.S. in Electronic and Electrical Engineering, Magna Cum Laude
- GPA: 3.71/4.30 overall (4.01/4.30 Upper)
- 03/1996 - 2/1999 **Seoul Science High School, Seoul, Korea**
- For gifted students in mathematics and sciences

PUBLICATIONS

- DAC'12 **Process Variation in Near-Threshold Wide SIMD Architecture**
- Sangwon Seo, Ronald Dreslinski, Mark Woh, **Yongjun Park**, Scott Mahlke, David Blaauw, Chaitali Chakrabarti, and Trevor Mudge
- Proc. 49th Design Automation Conference (DAC), June. 2012. (to appear)
- ASPLOS'12 **SIMD Defragmenter: Efficient ILP Realization on Data-parallel Architectures**
- **Yongjun Park**, Sangwon Seo, Hyunchul Park, Hyoun Kyu Cho, and Scott Mahlke
- Proc. 17th Intl. Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), March.2012 (to appear)
- CASES'10 **Resource Recycling: Putting Idle Resources to Work on a Composable Accelerator**
- **Yongjun Park**, Hyunchul Park, Scott Mahlke, and Sukjin Kim
- Proc. 2010 Intl. Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), Oct. 2010
- MICRO'09 **Polymorphic Pipeline Array: A Flexible Multicore Accelerator with Virtualized Execution for Mobile Multimedia Applications**
- Hyunchul Park, **Yongjun Park**, and Scott Mahlke
- Proc. 42nd Intl. Symposium on Microarchitecture (MICRO), Dec. 2009, pp. 370-380.

CASES'09 **CGRA Express: Accelerating Execution using Dynamic Operation Fusion**
- **Yongjun Park**, Hyunchul Park, and Scott Mahlke
- Proc. 2009 Intl. Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), Oct. 2009, pp. 271-280.

SASP' 09 **A Dataflow-centric Approach to Design Low Power Control Paths in CGRAs**
- Hyunchul Park, **Yongjun Park**, and Scott Mahlke
- Proc. 7th IEEE Symposium on Application Specific Processors (SASP), Jul. 2009, pp. 15-20.

ODES'09 **Reducing Control Power in CGRAs with Token Flow**
- Hyunchul Park, **Yongjun Park**, and Scott Mahlke
- 7th Workshop on Optimizations for DSP and Embedded Systems (ODES-7), March, 2009

PATENTS

07/2011 **Computing Apparatus and Method based on a Reconfigurable Single Instruction Multiple Data (SIMD) Architecture** (patent filed)

- Jaeun Park, Sukjin Kim, Scott Mahlke, and **Yongjun Park**

07/2011 **Compiling Apparatus and Method of a Multicore Device** (patent filed)

- Kiseok Kwon, Sukjin Kim, Scott Mahlke, and **Yongjun Park**

10/2009 **Processor with a Reconfigurable Architecture** (patent filed)

- Heejun Shim, Sukjin Kim, Hyunchul Park, Scott Mahlke, and **Yongjun Park**

WORK EXPERIENCE

01/2008 - Present **CCCP Research Group, University of Michigan, Ann Arbor, MI**

- *Graduate Student Research Assistant*

- Architecture optimization for Coarse-Grained Reconfigurable Architectures, SIMD, and GPU

- Compiler optimization for achieving high resource utilization for CGRAs, SIMD and GPU

06/2009 - 08/2009 **SAMSUNG Advanced Institute of Technology, Giheung, Korea**

- *Summer Intern*

- StreamIt-based frontend compiler implementation for polymorphic pipeline array

06/2008 - 07/2008 **SAMSUNG Advanced Institute of Technology, Giheung, Korea**

- *Summer Intern*

- Design space exploration of coarse grained reconfigurable architecture

07/2005 - 08/2005 **LG Electronics Inc., Seoul, Korea**

- *Summer Intern*

- Digital logic research and design for ASIC Projects by VHDL

01/2002 - 01/2005 **ALTECH (Airlink Technology), Seoul, Korea**

- *Full time researcher and engineer*

- 2 times Tape-out experiences for Arm Processor based ASIC Projects

- Digital logic design using Cadence and Synopsys Tools

- Embedded system application programming using the C language

PROJECT EXPERIENCE

07/2005 - 08/2005 **Camera Module ASIC Project at LG Electronics Inc.**

- Worked on FIR Filter logic for Camera Module by VHDL

- 04/2004 - 01/2005 **Media Player Project at ALTECH**
 - Programmed Media Player Firmware by C language
- 04/2003 - 03/2004 **ANS2 Project with Samsung Electronics Inc.**
 - ARM920T-based 200MHz Network Solution ASIC Chip of Residential Gateway Project supported by Korea Ministry of Commerce, Industry and Energy
 - Worked on fast Memory, ATA UDMA interface and peripheral logics
- 01/2002 - 03/2003 **ANS1 Project with Hynix Semiconductor Inc.**
 - ARM720T-based 67MHz Network Solution ASIC Chip of Residential Gateway Project supported by Korea Ministry of Commerce, Industry and Energy
 - Worked on fast Memory interface and peripheral logics

HONORS AND AWARDS

- 09/2007 - 08/2010 **Scholarship from Korea Industrial Technology Foundation for Overseas Studies**
 - A scholarship awarded to nationally 15 doctoral students
- 09/2005 **Scholarship for the Highest Honors at POSTECH**
 - A scholarship awarded to the top one student among all senior POSTECH EEE students.
- 02/1999 **A Prize for High Scholarship at Seoul Science High School**

SERVICES AND ACTIVITY

- Reviewer for:
- International Symposium on High Performance Computer Architecture (HPCA '10, 11)
 - International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS '10, 11)
 - International Symposium on Computer Architecture (ISCA '10, 11, 12)
 - Parallel Architectures and Compilation Techniques (PACT '10)
 - International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES '10)
 - International Symposium on Code Generation and Optimization (CGO '12)
 - Design, Automation and Test in Europe (DATE '10)
 - Design Automation Conference (DAC '11, 12)
 - IEEE Symposium on Application Specific Processors (SASP '11)
 - International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS '10)

CLASSES/SKILLS

- Univ. of Michigan - VLSI Design 1/2, Circuit Synthesis & Optimization, Computer Architecture, Digital Integrated Technology, Algorithms, Parallel Computer Architecture, Advanced Compiler, Linear Space Matrix Theory, Probability & Random Process
- POSTECH - Digital Logic Design, Computer Design, Digital Integrated Circuit Design, VLSI Analysis & Design Software, Embedded System Design
- Programming & Tools
- C, C++, JAVA, VHDL, Verilog HDL, StreamIt, Trimaran(OpenImpact), LLVM
 - Pspice, Hspice, Smartspice, Synopsys Tools, Cadence NC-verilog