

Wei Lu

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Wei D. Lu is a Professor in the Electrical Engineering and Computer Science department at the University of Michigan. He received B.S. in physics from Tsinghua University, Beijing, China in 1996, and Ph.D. in physics from Rice University, Houston, TX in 2003, followed by a postdoctoral research fellow position at Harvard University, Cambridge, MA from 2003-2005. He joined the faculty of the University of Michigan in 2005. Prof. Lu's research interest includes resistive-random access memory (RRAM), memristor-based logic circuits, neuromorphic computing systems, aggressively scaled transistor devices, and electrical transport in low-dimensional systems. To date Prof. Lu has published over 200 journal and conference articles, with more than 38,000 citations and an H-index of 89 (Google Scholar, <https://scholar.google.com/citations?user=pPInY4UAAAAAJ&hl=en>). He is a recipient of the NSF CAREER award, co-founder of Crossbar Inc and MemryX Inc., and an IEEE Fellow.

Professional Preparation

Tsinghua University, China	Physics	B.S.	1996
Rice University, Houston, TX	Physics	Ph.D.	2003
Harvard University, Cambridge, MA	Chemistry	Postdoc	2003-05

Appointments

2005-present **Assistant Professor, Associate Professor, Professor, Electrical Engineering and Computer Science Department, the University of Michigan**

2016-present **Director, Lurie Nanofabrication Facility, University of Michigan**

- Co-founder, CTO, MemryX Inc, a semiconductor chip company headquartered in Ann Arbor that offers high-performance and energy efficient edge AI chips.
- Co-founder, Crossbar Inc, a semiconductor company based in Silicon Valley that offers high density and high-performance RRAM-based memory technologies.
- Founding Editor-in-Chief, *NPJ Unconventional Computing*, Nature Portfolio Journals
- Currently advising 7 Ph.D students; graduated 22 Ph.Ds and advised 9 PostDocs
- First experimental study on memristor-based system that exhibits key synaptic functionalities for neuromorphic applications
 - Jo et al. "Nanoscale Memristor Device as Synapse in Neuromorphic Systems," *Nano Lett.*, **10**, 1297-1301 (2010). (over 4000 citations)
- First memristor/RRAM computing chip
 - Cai et al. "A Fully Integrated Reprogrammable Memristor-CMOS System for Efficient Multiply-Accumulate Operations", *Nature Electronics*, **2**, 290-299 (2019). (Cover Article)
- Efficient in-memory processing systems based on memristor/RRAM fabric
 - Sheridan et al. "Sparse Coding with Memristor Networks," *Nature Nanotechnology*, **12**, 784-789 (2017); Zidan, et al. "A general memristor-based partial differential equation solver", *Nature Electronics* **1**, 411-420 (2018)
- Memristor networks for temporal data processing
 - Du et al., "Reservoir Computing Using Dynamic Memristors for Temporal Information Processing," *Nature Communications*, **8**: 2204, (2017); Moon et al., "Temporal data classification and forecasting using a memristor-based reservoir computing system", *Nature Electronics* **2**, 480-487 (2019)
- High-density memory based on resistive-switching devices

- Jo et al. “High-Density Crossbar Arrays Based on a Si Memristive System”, *Nano Lett.* **9**, 870-874 (2009); Jo et al. “CMOS Compatible Nanoscale Nonvolatile Resistance Switching Memory,” S. Jo, and W. Lu, *Nano Lett.* **8**, 392-397 (2008).
 - Demonstrated vertical high-performance nanowire transistors and Si-Ge heterojunction Esaki tunnel diodes; Demonstrated nanowire-based transparent TFTs; Demonstrated nanowire-based nanoelectromechanical devices
- 2003-05, Postdoctoral fellow, Department of Chemistry and Chemical Biology, Harvard University**
- Demonstrated high-performance electronic devices based on radial core/shell nanowire heterostructures
 - Xiang* and Lu* et al. “Ge/Si nanowire heterostructures as high-performance field-effect transistors”, *Nature.* **441**, 489-493 (2006).
 - Demonstrated coherent charge transport through semiconductor nanowires; Developed metal/semiconductor nanowire axial heterostructures through a solid-state reaction process
- 1996-03, Graduate Research Assistant, Department of Physics and Astronomy, and Center for Nanoscale Science and Technology, Rice University**
- Developed the first system to directly observe electron tunneling in nanoscale devices in real-time
 - Lu et al., “Real-time detection of electron tunneling in a quantum dot”, *Nature.* **423**, 422-425 (2003).
 - Developed a strongly coupled single-electron transistor/quantum dot system
 - Developed controlled assembly techniques for carbon-nanotubes

Awards

- 2023 IEEE Circuits and Systems Society Transactions on Circuits and Systems Darlington Best Paper Award
- Ted Kennedy Family Faculty Team Excellence Award, University of Michigan, 2022
- Distinguished University Innovator Award, University of Michigan, 2022
- Best invited paper, IEEE Custom Integrated Circuits Conference (CICC) 2018
- IEEE Fellow, 2018
- 2016-2017 David E. Liddle Research Excellent Award
- 2014-2015 Rexford E. Hall Innovation Excellence Award
- 2012-2013 EECS Outstanding Achievement Award (2013)
- NSF CAREER Award. (2010)
- Wilson Award, to the graduate student for most outstanding Ph.D. thesis in Physics and Astronomy, Rice University. (2003)
- Chuoke Award, to the 2nd or 3rd year graduate student in Physics for outstanding academic and research performance, Rice University. (1999)
- Chuoke Award, to the 2nd or 3rd year graduate student in Physics for outstanding academic and research performance, Rice University. (1998)
- Liqing Academic Award, to the highest-ranked junior or senior student in Physics for most outstanding academic performance, Tsinghua University. (1995)
- Outstanding Student Award, given to undergraduate students for excellent academic performance, Tsinghua University. (1992, 1993, 1994, 1996)

Professional Service

- Founding Editor-in-Chief, Unconventional Computing, NPJ Series
- Associate Editor, *Nanoscale* (2009-2017).
- Member, ITRS Emerging Research Device Working Group (2011-2016)
- Program committee, novel devices, IEEE International Electron Devices Meeting (IEDM) 2014-2015. Program committee, IEEE Non-Volatile Memory Technology Symposium 2014-present.

- Organizer, CAS-FAST symposium at The IEEE International Symposium on Circuits and Systems (ISCAS 2014), the 4th Symposium on Memristors and Memristive Systems (2014) and the 3rd Symposium on Memristors and Memristive Systems (2012).
- Reviewer for over 30 journals including Nature, Nature Materials, Nature Nanotechnology, Nature Communications, Nano Letters, Journal of the American Chemical Society, Advanced Materials, IEEE Electron Device Letters, IEEE Transactions on Electron Devices, IEEE Transactions on Nanotechnology, IEEE Transactions on Microwave Theory and Techniques, Applied Physics Letters, Journal of Applied Physics, Nanotechnology, Small, Chemical Physics Letters, Journal of Vacuum Science and Technology, Journal of Electronic Materials, Journal of Physics, Solid State Communications, Physics Letters A, Organic Electronics Letters, Materials Today and Solid State Electronics.
- Panelist for NSF CAREER, NIRT, EMT, SBIR and EPDT proposals.
- Reviewer for DOE, AFOSR and ARO proposals.
- Program Committee, 1st IEEE International Workshop on Design and Test of Nano Devices, Circuits and Systems (NDCS) 2009. IEEE Nanotechnology Materials and Devices Conference 2009.
- Member, IEEE Molecular, Biological and Multi-Scale Communications Technical Committee (MBMC-TC), 2017-present
- Member, IEEE Nanotechnology Council Nano Energy, Environment, and Safety (NTC NEES)

University Service

- Director, Lurie Nanofabrication Facility (2017-19)
- ECE Executive Committee
- EECS Grad Fellowships
- EE UG Honors Committee

Books

“Semiconductor Nanowires”, Editor(s): Wei Lu, Jie Xiang, RSC Publishing, 2014.

Book Chapters

- [1] “Memristors and Memristive Devices for Neuromorphic Computing”, Patrick Sheridan and Wei D. Lu, in *Handbook of Memristor Networks*, L. Chua eds, Springer, 2019
- [2] “Memristive Devices: Switching Effects, Modeling, and Applications”, Yuchao Yang, Ting Chang and Wei Lu, in *Memristors and Memristive Systems*, R. Tetzlaff eds., Springer, 2014.
- [3] “Memristors and Memristive Devices for Neuromorphic Computing”, Patrick Sheridan and Wei Lu, in *Memristor Networks*, A. Adamatzky and L. Chua eds., Springer, 2014.
- [4] “Resistive-RAM Based on Amorphous Films”, Y. Yang, and W. Lu, in *Handbook of Nonvolatile Memories: Materials, Devices and Applications*, T. Y. Tseng and S. M. Sze eds., American Scientific Publishers, 2011.
- [5] “Hierarchical 3D Nanostructure Organization for Next Generation Devices”, E. N. Dattoli, and W. Lu, in *Three-Dimensional Nanoarchitectures: Designing Next-Generation Devices*, Z.L.

- Wang eds., Springer, 2010.
- [6] “Nanoelectronics from the Bottom Up”, W. Lu and C. M. Lieber, in *World Scientific Series in Nanoscience and Nanotechnology*, M. Reed eds., World Scientific Publishers, 2009.

Journal Publications

- [1] "Training Spiking Neural Networks Using Lessons From Deep Learning," Jason K Eshraghian, Max Ward, Emre O Neftci, Xinxin Wang, Gregor Lenz, Girish Dwivedi, Mohammed Bennamoun, Doo Seok Jeong, Wei D Lu, *Proceedings of the IEEE*, vol. 111, no. 9, pp. 1016-1054, Sept. 2023, doi: 10.1109/JPROC.2023.3308088.
- [2] “Side-Channel Attack Analysis on In-Memory Computing Architectures,” Z. Wang, F. -h. Meng, Y. Park, J. K. Eshraghian and W. D. Lu, *IEEE Transactions on Emerging Topics in Computing*, doi: 10.1109/TETC.2023.3257684. (2023)
- [3] "Exploring Compute-in-Memory Architecture Granularity for Structured Pruning of Neural Networks," F. -H. Meng, X. Wang, Z. Wang, E. Y. -J. Lee and W. D. Lu, *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 12, no. 4, pp. 858-866, (2022) doi: 10.1109/JETCAS.2022.3227471.
- [4] "Gradient-Based Neuromorphic Learning on Dynamical RRAM Arrays," P. Zhou, D. -U. Choi, W. D. Lu, S. -M. Kang and J. K. Eshraghian, *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 12, no. 4, pp. 888-897, (2022), doi: 10.1109/JETCAS.2022.3224071.
- [5] “Columnar Learning Networks for Multisensory Spatiotemporal Learning,” Yoo, S., Park, Y., Wang, Z., Wu, Y., Medepalli, S., Thio, W. and Lu, W.D. (2022), *Adv. Intell. Syst.*, 4: 2200179. <https://doi.org/10.1002/aisy.202200179>
- [6] "RM-NTT: An RRAM-Based Compute-in-Memory Number Theoretic Transform Accelerator," Y. Park, Z. Wang, S. Yoo and W. D. Lu, *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, vol. 8, no. 2, pp. 93-101, (2022), doi: 10.1109/JXCDC.2022.3202517.
- [7] “Memristive technologies for data storage, computation, encryption, and radio-frequency communication” Mario Lanza et al., *Science*, **376**, 9979 (2022).DOI:10.1126/science.abj9979
- [8] “Dynamical memristors for higher-complexity neuromorphic computing”, Suhas Kumar, Xinxin Wang, John Paul Strachan, Yuchao Yang, Wei D Lu, *Nature Reviews Materials*, **7**, 575–591 (2022)
- [9] “Physical unclonable function systems based on pattern transfer of fingerprint-like patterns”, Ziyu Wang, Xiaojian Zhu, Supreet Jeloka, Brian Cline, Wei D Lu, *IEEE Electron Device Letters*, 10.1109/LED.2022.3154655. (2022)
- [10] “Tuning Resistive Switching Behavior by Controlling Internal Ionic Dynamics for Biorealistic Implementation of Synaptic Plasticity”, Yoo, S., Wu, Y., Park, Y., & Lu, W. D., *Advanced Electronic Materials*, **8**, 2101025 (2022). <https://doi.org/https://doi.org/10.1002/aelm.202101025>
- [11] “Device Variation Effects on Neural Network Inference Accuracy in Analog In-Memory Computing Systems”, Wang, Q., Park, Y., & Lu, W. D, *Advanced Intelligent Systems*, **4**: 2100199 (2022). <https://doi.org/https://doi.org/10.1002/aisy.202100199>
- [12] “TAICHI: A Tiled Architecture for In-Memory Computing and Heterogeneous Integration”,

- Wang, X., Pinkham, R., Zidan, M. A., Meng, F.-H., Flynn, M. P., Zhang, Z., & Lu, W. D. , *IEEE Transactions on Circuits and Systems II: Express Briefs*, 69(2), 559–563. (2022) <https://doi.org/10.1109/TCSII.2021.3097035>
- [13] “Hierarchical architectures in reservoir computing systems”, Moon, J., Wu, Y., & Lu, W. D., *Neuromorphic Computing and Engineering*, 1(1), 014006 (2021). <https://doi.org/10.1088/2634-4386/ac1b75>
- [14] “Investigating Selectorless Property within Niobium Devices for Storage Applications”, Chen, P.-H., Lin, C.-Y., Chang, T.-C., Eshraghian, J. K., Chao, Y.-T., Lu, W. D., & Sze, S. M., *ACS Applied Materials & Interfaces*, 14(1), 2343–2350. <https://doi.org/10.1021/acsami.1c20460> (2022)
- [15] “Memristor-Based Binarized Spiking Neural Networks: Challenges and Applications”, Eshraghian, J. K., Wang, X., & Lu, W. D. *IEEE Nanotechnology Magazine*, 2–11. <https://doi.org/10.1109/MNANO.2022.3141443> (2022)
- [16] “How to Build a Memristive Integrate-and-Fire Model for Spiking Neuronal Signal Generation”, Sung Mo Kang, Donguk Choi, Jason K Eshraghian, Peng Zhou, Jieun Kim, Bai-Sun Kong, Xiaojian Zhu, Ahmet Samil Demirkol, Alon Ascoli, Ronald Tetzlaff, Wei D Lu, Leon O Chua, *IEEE Transactions on Circuits and Systems I: Regular Papers*, 68(12), 4837-4850. doi:10.1109/TCSI.2021.3126555 (2021)
- [17] “Neural connectivity inference with spike-timing dependent plasticity network”. *Science China Information Sciences*, 64(6). doi:10.1007/s11432-021-3217-0 (2021)
- [18] “Memristors Based on (Zr, Hf, Nb, Ta, Mo, W) High-Entropy Oxides”. Minhyung Ahn, Yongmo Park, Seung Hwan Lee, Sieun Chae, Jihang Lee, John T Heron, Emmanouil Kioupakis, Wei D Lu, Jamie D Phillips, *Advanced Electronic Materials*, 7(5). doi:10.1002/aelm.202001258 (2022)
- [19] “Memristive Stochastic Computing for Deep Learning Parameter Optimization”, Lammie, C., Eshraghian, J. K., Lu, W. D., & Azghadi, M. R., *IEEE Transactions on Circuits and Systems II: Express Briefs*, 68(5), 1650-1654. doi:10.1109/TCSII.2021.3065932
- [20] “Neural Functional Connectivity Reconstruction with Second-Order Memristor Network”, Yuting Wu, John Moon, Xiaojian Zhu, Wei D. Lu, *Advanced Intelligent Systems*, 2021, (<https://doi.org/10.1002/aisy.202000276>)
- [21] “Adaptive Synaptic Memory via Lithium Ion Modulation in RRAM Devices”, ChihYang Lin, Jia Chen, Po-Hsun Chen, Ting-Chang Chang, Yuting Wu, Jason K Eshraghian, John Moon, Sangmin Yoo, Yu-Hsun Wang, Wen-Chung Chen, Zhi-Yang Wang, Hui-Chun Huang, Yi Li, Xiangshui Miao, Wei D. Lu, Simon M. Sze, *Small* **16** (42), 2003964 (2020)
- [22] “Power-efficient combinatorial optimization using intrinsic noise in memristor Hopfield neural networks,” Fuxi Cai, Suhas Kumar, Thomas Van Vaerenbergh, Xia Sheng, Rui Liu, Can Li, Zhan Liu, Martin Foltin, Shimeng Yu, Qiangfei Xia, J Joshua Yang, Raymond Beausoleil, Wei D Lu, John Paul Strachan, *Nature Electronics* **3** (7), 409-418 (2020)
- [23] “A high-speed MIM resistive memory cell with an inherent vanadium selector,” Chih-Yang Lin, Yi-Ting Tseng, Po-Hsun Chen, Ting-Chang Chang, Jason K Eshraghian, Qiwen Wang, Qi Lin, Yung-Fang Tan, Mao-Chou Tai, Wei-Chun Hung, Hui-Chun Huang, Wei D Lu, Simon M. Sze, *Applied Materials Today*, **21**, 100848 (2020)

- [24] “A crossbar-based in-memory computing architecture”, X. Wang, M.A. Zidan, W.D. Lu, *IEEE Transactions on Circuits and Systems I: Regular Papers* **67** (12), 4224-4232 (2020)
- [25] “Memristor networks for real-time neural activity analysis”, Xiaojian Zhu, Qiwen Wang & Wei D. Lu, *Nature Communications*, **11**, 2439 (2020) (<https://doi.org/10.1038/s41467-020-16261-1>)
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- [27] “Near infrared neuromorphic computing via upconversion-mediated optogenetics”, Y Zhai, Y Zhou, X Yang, F Wang, W Ye, X Zhu, D She, WD Lu, ST Han, *Nano Energy*, **67**, 104262 (2020)
- [28] “Nanoscale resistive switching devices for memory and computing applications”, Lee, S.H., Zhu, X. & Lu, W.D. *Nano Res.* **13** (5), 1228-1243 (2020). <https://doi.org/10.1007/s12274-020-2616-0>
- [29] “Temporal data classification and forecasting using a memristor-based reservoir computing system”, John Moon, Wen Ma, Jong Hoon Shin, Fuxi Cai, Chao Du, Seung Hwan Lee & Wei D. Lu, *Nature Electronics* **2**, 480–487 (2019)
- [30] “A Fully Integrated Reprogrammable Memristor-CMOS System for Efficient Multiply-Accumulate Operations”, Fuxi Cai, Justin M. Correll, Seung Hwan Lee, Yong Lim, Vishishtha Bothra, Zhengya Zhang, Michael P. Flynn, and Wei D. Lu, *Nature Electronics*, **2**, 290–299 (2019). (Cover Article)
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- [32] “Charge Transition of Oxygen Vacancies during Resistive Switching in Oxide-Based RRAM”, Jihang Lee, William Schell, Xiaojian Zhu, Emmanouil Kioupakis, and Wei D. Lu, *ACS Appl. Mater. Interfaces*, **11**, 11579-11586 (2019)
- [33] “Ionic modulation and ionic coupling effects in MoS₂ devices for neuromorphic computing”, Xiaojian Zhu, Da Li, Xiaogan Liang, & Wei D. Lu, *Nature Materials*, **18**, 141–148 (2019).
- [34] “Recommended methods to study resistive switching devices”, Mario Lanza, et al., *Advanced Electronic Materials*, **5**, 1800143 (2019)
- [35] “Self-Limited and Forming-Free CBRAM Device with Double Al₂O₃ ALD Layers”, Jong Hoon Shin, Qiwen Wang, Wei D Lu, *IEEE Electron Device Letters*, **39**, 1512-1515 (2018)
- [36] “Neuromorphic Computing Using Memristor Crossbar Networks: A Focus on Bio-Inspired Approaches”, YeonJoo Jeong, Wei Lu, *IEEE Nanotechnology Magazine*, **12**, 6-18 (2018)
- [37] “A general memristor-based partial differential equation solver”, Mohammed A. Zidan, YeonJoo Jeong, Jihang Lee, Bing Chen, Shuo Huang, Mark J. Kushner & Wei D. Lu, *Nature Electronics* **1**, 411–420 (2018)
- [38] “K-means Data Clustering with Memristor Networks,” YeonJoo Jeong, Jihang Lee, John Moon, Jong Hoon Shin, and Wei D. Lu, *Nano Lett.*, **18** (7), 4447–4453 (2018)
- [39] “Neuromorphic computing with memristive devices”, Wen Ma, Mohammed A Zidan, Wei D Lu, *Science China Information Sciences*, **61** (6), 060422 (2018)
- [40] “Parasitic Effect Analysis in Memristor-Array-Based Neuromorphic Systems,” Y.J. Jeong, M.A. Zidan, W.D. Lu, *IEEE Transactions on Nanotechnology* **17** (1), 184-193 (2018).
- [41] “Optogenetics-Inspired Tunable Synaptic Functions in Memristors”, Xiaojian Zhu and Wei D. Lu, *ACS Nano*, **12** (2), pp 1242–1249 (2018)

- [42] “The Future of Electronics Based on Memristive Systems”, Mohammed A. Zidan, John Paul Strachan & Wei D. Lu, *Nature Electronics*, **1**, 22–29 (2018)
- [43] “MoS₂ Memristors Exhibiting Variable Switching Characteristics toward Biorealistic Synaptic Emulation”, D Li, B Wu, X Zhu, J Wang, B Ryu, WD Lu, W Lu, X Liang, *ACS Nano* **12** (9), 9240-9252 (2018).
- [44] “Reservoir computing using dynamic memristors for temporal information processing”, C. Du, F. Cai, M. A Zidan, W. Ma, S.H. Lee, and Wei D. Lu, *Nature Communications* **8**, 2204 (2017) doi:10.1038/s41467-017-02337-y
- [45] “On-Demand Reconfiguration of Nanomaterials: When Electronics Meets Ionics”, Jihang Lee, Wei D. Lu, *Advanced Materials*, **30**, 1702770 (2018)
- [46] “Memristive computing devices and applications,” M.A. Zidan, A. Chen, G. Indiveri, W.D. Lu, *Journal of Electroceramics* **39** (1-4), 4-20 (2017)
- [47] “Iodine vacancy redistribution in organic–inorganic halide perovskite films and resistive switching effects,” X. Zhu, J. Lee, W.D. Lu, *Advanced Materials* **29**, 1700527 (2017)
- [48] “Field-Programmable Crossbar Array (FPCA) for Reconfigurable Computing”, Mohammed A. Zidan, YeonJoo Jeong, Jong Hoon Shin, Chao Du, Zhengya Zhang, and Wei D. Lu, *IEEE Trans Multi-Scale Comp Sys*, **4**, 698-710 (2018)
- [49] “Sparse Coding with Memristor Networks”, Patrick M. Sheridan, Fuxi Cai, Chao Du, Wen Ma, Zhengya Zhang & Wei D. Lu, *Nature Nanotechnology*, **12**, 784–789 (2017)
- [50] “Temporal Learning Using Second-Order Memristors,” M.A. Zidan, Y.J. Jeong, W.D. Lu, *IEEE Transactions on Nanotechnology*, **16** (4), 721-723 (2017)
- [51] "Experimental Demonstration of Feature Extraction and Dimensionality Reduction Using Memristor Networks," S. Choi, J. H. Shin, J. Lee, P. Sheridan, and W. D. Lu, *Nano Letters*, **17**, 3113–3118 (2017).
- [52] “Electronic and optical properties of oxygen vacancies in amorphous Ta₂O₅ from first principles,” Jihang Lee, Wei D. Lu and Emmanouil Kioupakis, *Nanoscale*, **9**, 1120-1127 (2017).
- [53] “Ge nanowire photodetector with high photoconductive gain epitaxially integrated on Si substrate,” U. Otuonye, H.W. Kim, W.D. Lu, *Applied Physics Letters*, **110** (17), 173104 (2017)
- [54] “Emulation of synaptic metaplasticity in memristors”, Xiaojian Zhu, Chao Du, YeonJoo Jeong, Wei D. Lu, *Nanoscale*, **9** (1), 45-51 (2017)
- [55] “Progress in the Characterizations and Understanding of Conducting Filaments in Resistive Switching Devices”, Yuchao Yang, Wei D. Lu, *IEEE Transactions on Nanotechnology* **15** (3), 465-472 (2016)
- [56] “Tuning Ionic Transport in Memristive Devices by Graphene with Engineered Nanopores”, Jihang Lee, Chao Du, Kai Sun, Emmanouil Kioupakis, and Wei D. Lu, *ACS Nano*, **10** (3), pp 3571–3579 (2016).
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- [58] “Single-Readout High-Density Memristor Crossbar”, MA Zidan, H Omran, R Naous, A Sultan, HAH Fahmy, WD Lu, KN Salama, *Scientific Reports* **6**, 18863 (2016)
- [59] “Nanoscale electrochemistry using dielectric thin films as solid electrolytes”, Ilia Valov, Wei D. Lu, *Nanoscale* **8** (29), 13828-13837 (2016)
- [60] “Very Low-Programming-Current RRAM With Self-Rectifying Characteristics”, J. Zhou, F. Cai, Q. Wang, B. Chen, S. Gaba, W. D. Lu, *IEEE Electron Device Letters*, **37**, 404-407 (2016)
- [61] “Vertical Ge/Si Core/Shell Nanowire Junctionless Transistor”, Lin Chen, Fuxi Cai, Ugo Otuonye, and Wei D. Lu, *Nano Lett.*, **16** (1), 420–426 (2016).
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- [64] “Utilizing multiple state variables to improve the dynamic range of analog switching in a memristor”, YeonJoo Jeong, Sungho Kim, Wei D Lu, *Appl. Phys. Lett.* **107**, 173105 (2015).
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- [66] “Biorealistic Implementation of Synaptic Functions with Oxide Memristors through Internal Ionic Dynamics,” Chao Du, Wen Ma, Ting Chang, Patrick Sheridan, Wei D. Lu, *Advanced Functional Materials*, **25**, 4290–4299, (2015)
- [67] “Data Clustering using Memristor Networks”, ShinHyun Choi, Patrick Sheridan, Wei D. Lu, *Scientific Reports*, **5**:10492 (2015).
- [68] “An Optoelectronic Resistive Switching Memory with Integrated Demodulating and Arithmetic Functions” , Hongwei Tan, Gang Liu, Xiaojian Zhu, Huali Yang, Bin Chen, Xinxin Chen, Jie Shang, Wei D Lu, Yihong Wu, Runwei Li, *Advanced Materials*, **27**, 2797-2803, (2015)
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- [76] “Electrochemical dynamics of nanoscale metallic inclusions in dielectrics”, Yuchao Yang, Peng Gao, Linze Li, Xiaoqing Pan, Stefan Tappertzhofen, ShinHyun Choi, Rainer Waser, Ilia Valov, Wei D. Lu, *Nature Communications*, **5**, 4232 (2014)
- [77] “Crossbar RRAM Arrays: Selector Device Requirements During Read Operation”, Jiantao Zhou, Kuk-Hwan Kim, and Wei Lu, *IEEE Transactions On Electron Devices*, **61** (5), 1369-1376 (2014).
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Conference Proceedings

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- "Navigating Local Minima in Quantized Spiking Neural Networks," J. K. Eshraghian, C. Lammie, M. R. Azghadi and W. D. Lu, 2022 IEEE 4th International Conference on Artificial Intelligence Circuits and Systems (AICAS), Incheon, Korea, Republic of, 2022, pp. 352-355, doi: 10.1109/AICAS54282.2022.9869966.
- "An 8-bit 20.7 TOPS/W Multi-Level Cell ReRAM-based Compute Engine," J. M. Correll et al., " 2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), Honolulu, HI, USA, 2022, pp. 264-265, doi: 10.1109/VLSITechnologyandCir46769.2022.9830490.
- "Design Space Exploration of Dense and Sparse Mapping Schemes for RRAM Architectures." Lammie, C., Eshraghian, J. K., Li, C., Amirsoleimani, A., Genov, R., Lu, W. D., & Azghadi, M. R. (2022). In Proceedings - IEEE International Symposium on Circuits and Systems Vol. 2022-May (pp. 1107-1111). doi:10.1109/ISCAS48785.2022.9937207
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- "RRAM-enabled AI Accelerator Architecture", Wang, X., Wu, Y., & Lu, W. D., In 2021 IEEE International Electron Devices Meeting (IEDM) (p. 12.2.1-12.2.4). <https://doi.org/10.1109/IEDM19574.2021.9720543> (invited)
- "Device non-ideality effects and architecture-aware training in RRAM In-memory computing modules", Wang, Q., Park, Y., & Lu, W. D., In Proceedings - IEEE International Symposium on Circuits and Systems Vol. 2021-May. doi:10.1109/ISCAS51556.2021.9401307 (2021)
- "Deep Neural Network Mapping and Performance Analysis on Tiled RRAM Architecture," Xinxin Wang, Qiwen Wang, Fan-Hsuan Meng, Seung Hwan Lee, Wei D Lu, 2nd IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS), 141-144, 2020
- "A Deep Neural Network Accelerator Based on Tiled RRAM Architecture", Xinxin Wang, Qiwen Wang, Seung Hwan Lee, Fan-Hsuan Meng, and Wei D. Lu IEEE International Devices Conference (IEDM), 14.4.1-14.4.4, 2019.
- "Hardware Acceleration of Simulated Annealing of Spin Glass by RRAM Crossbar", Jong Hoon Shin, YeonJoo Jeong, Mohammed A. Zidan, Qiwen Wang, and Wei D. Lu, IEEE International Devices Conference (IEDM), 2018.

- “RRAM fabric for neuromorphic and reconfigurable compute-in-memory systems”, M.A. Zidan, W.D. Lu, IEEE Custom Integrated Circuits Conference (CICC), 2018, 1-8 (invited, Best Paper)
- “Feature extraction and analysis using memristor networks”, F Cai, WD Lu, 2018 IEEE International Symposium on Circuits and Systems (ISCAS).
- “Epsilon-greedy strategy for online dictionary learning with realistic memristor array constraints”, F. Cai, W.D. Lu, 2017 IEEE/ACM International Symposium on Nanoscale Architectures (NANOARC)
- “Hybrid neural network using binary RRAM devices”, M.A. Zidan, Y.J. Jeong, W.D. Lu, 2017 IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)
- “Device Nonideality Effects on Image Reconstruction Using Memristor Arrays”, Wen Ma, Fuxi Cai, Chao Du, Yeonjoo Jeong, Mohammed Zidan and Wei D. Lu, Electron Devices Meeting (IEDM), 2016 IEEE International. 16.7.1-16.7.4
- “Efficient in-memory computing architecture based on crossbar arrays”, Bing Chen, Fuxi Cai Wen Ma and Wei D. Lu, Electron Devices Meeting (IEDM), 2015 IEEE International. 17.5.1-17.5.4
- “Characterizations and Understanding of Conducting Filaments in Resistive Switching Devices”, Yuchao Yang, Wei D. Lu, 15th International Conference on Nanotechnology, IEEE (IEEE Nano), July 2015 (invited).
- “Defect Considerations for Robust Sparse Coding Using Memristor Arrays,” Patrick Sheridan and Wei D. Lu, IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH 15), Boston, MA, July 2015.
- “FPAA/Memristor Hybrid Computing Infrastructure,” Mika Laiho, Jennifer O Hasler, Jiantao Zhou, Chao Du, Wei Lu, Eero Lehtonen, Jussi H Poikonen, Circuits and Systems (ISCAS), 2015 IEEE International Symposium on, 62, 906-915.
- “3D-stackable crossbar resistive memory based on Field Assisted Superlinear Threshold (FAST) selector,” SH Jo, T Kumar, S Narayanan, WD Lu, H Nazarian, Electron Devices Meeting (IEDM), 2014 IEEE International, 6.7. 1-6.7. 4 (2014)
- “Pattern recognition with memristor networks,” P Sheridan, W Ma, W Lu, Circuits and Systems (ISCAS), 2014 IEEE International Symposium on, 1078-1081
- “Memristive devices for stochastic computing”, S Gaba, P Knag, Z Zhang, W Lu, Circuits and Systems (ISCAS), 2014 IEEE International Symposium on, 2592-2595
- “Analog signal processing on a FPAA/memristor hybrid circuit”, M Laiho, E Lehtonen, JO Hasler, J Zhou, C Du, W Lu, JH Poikonen, Circuits and Systems (ISCAS), 2014 IEEE International Symposium on, 2265-2268
- “Modeling and implementation of oxide memristors for neuromorphic applications”, Ting Chang, Patrick Sheridan, and Wei Lu. International Workshop on Cellular Nanoscale Networks and their Applications, 2012. (invited)

- “Memristive analog arithmetic within cellular arrays”, Mika Laiho, Eero Lehtonen, Wei Lu, 2012 IEEE International Symposium on Circuits and Systems (ISCAS), pp. 2665-2668, May 2012.
- “Improvement of RRAM Device Performance Through On-Chip Resistors”, Siddharth Gaba, Shinhyun Choi, Patrick Sheridan, Ting Chang, Yuchao Yang, Wei Lu, MRS Proceedings, **1430**, pp. 177-182, April 2012.
- “Time-Dependency of the Threshold Voltage in Memristive Devices”, E. Lehtonen, J. Poikonen, M. Laiho, and W. Lu, ISCAS 2011, Rio, June 2011.
- “Ultrafast Optical-Pump Terahertz-Probe Spectroscopy of Oriented Ge and Ge/Si Core/Shell Nanowires”, Momchil T Mihnev, Wayne Fung, Wei Lu, Theodore B Norris, Quantum Electronics and Laser Science Conference, May 2011.
- “Two-Terminal Resistive Switches (Memristors) for Memory and Logic Applications”, W. Lu, K.-H. Kim, T. Chang, and S. Gaba, 16th Asia and South Pacific Design Automation Conference, ASP-DAC 2011, Tokyo, January 2011, (invited).
- “Si Memristive Devices Applied to Memory and Neuromorphic Circuits”, Wei Lu, The IEEE International Symposium on Circuits and Systems, ISCAS 2010, Paris, June 2010, pp. 3333.1 (invited)
- “Nanowire Based Electronics: Challenges and Prospects”, International Electronic Device Meeting (IEDM), December 2009. (invited)
- “Experimental, Modeling and Simulation Studies of Nanoscale Resistance Switching Devices”, Sung Hyun Jo, Kuk-Hwan Kim, Ting Chang, Siddharth Gaba and Wei Lu, IEEE Nano 2009: the 9th International Conference on Nanotechnology, Genoa, Italy, July 2009.
- “Megahertz Frequency Characterization of Transparent Nanowire-based Thin-film Transistors”,
- Eric N. Dattoli, Kuk-Hwan Kim, Seok-Youl Choi, and Wei Lu, IEEE NMDC 2009: IEEE Nanotechnology Materials and Devices Conference 2009, Traverse City, June 2009. (invited)
- “Nanowire Devices and Their Applications to Displays”, E. N. Dattoli, K. H. Kim, and W. Lu, 15th Annual Symposium on Vehicle Displays, D Society for Information Display, Dearborn, October 2008. (invited)
- “Si-Based Two-Terminal Resistive Switching Nonvolatile Memory”, S. Jo and W. Lu, Proceedings of IEEE-ICSICT 08, The 9th International Conference on Solid-State and Integrated-Circuit Technology, Beijing, October 2008. 20-23 Oct. 2008 pp. 913 – 916. (invited)
- “Nanowire-Based High Speed Transparent and Flexible Thin-Film Transistor Devices”, E. N. Dattoli, K. Baler, W. Lu, Proceedings of MicroNano08, MicroNano2008-70328, Hong Kong, June 2008.
- “Nonvolatile Resistive Switching Behavior in Metal/Amorphous Silicon/Crystalline Silicon Junctions,” S. Jo, and W. Lu, Mat. Res. Soc. Proc., April 2007, vol. 997, pp. 153-158.

- “Versatile Metal Oxide Nanowire Devices Achieved via Controlled Doping,” E. N. Dattoli, Q. Wan and W. Lu, Mat. Res. Soc. Proc., April 2007, 1018-EE11-06.
- “Ag/a-Si:H/c-Si Resistive Switching Nonvolatile Memory Devices,” S. Jo, and W. Lu, IEEE NMDC 2006: IEEE Nanotechnology Materials and Devices Conference 2006, Proceedings, vol. 1. pp. 116-117, October 2006, Gyeongju, Korea.
- “Real-Time Electron Counting Studies on Charge Fluctuations in a Semiconductor Quantum Dot”, W. Lu, Proc. SPIE, May 2005, 5843: 124-140. (invited)

Invited Presentations and Seminars

“Intelligent computing based on device and material dynamics”, (Keynote) Neuromorphic Materials, Devices, Circuits and Systems (NeuMatDeCaS), January 2023.

“Intelligent Computing Enabled by Memristive Systems”, (Keynote) MEMRISYS 2022 Workshop, November 2022.

“In-memory and Intelligent Computing Systems Enabled by Emerging Memory Devices, Microelectronics symposium, Center for Integrated Nanotechnologies (CINT), LANL, September 2022.

“Engineering memristive devices for neuromorphic computing”, 20th International Symposium on the Physics of Semiconductors and Applications (ISPSA 2022), July 2022.

“Scalable design considerations for RRAM-based in-memory computing systems”, Design Automation Conference, DAC2022, July 2022.

“Intelligent Computing based on Device and Material Dynamics”, Intelligent Machines? – Self-organized Nonlinear Dynamics of Machines across Scales Workshop, June 2022.

“RRAM-enabled AI Accelerator Architecture”, 2021 International Electron Device Meeting, IEDM2021, December 2021.

“Neuromorphic Computing based on Memristive Systems”, Innovation Forum on Intelligent Computing, Science/Science Robotics/AAAS, November 2021.

“Modular Memristive Crossbar Architectures and Dynamic Memristive Networks”, International Conference on Memristive Materials, Devices & Systems (MEMRISYS 2021), November 2021 (Keynote).

“Neuromorphic Computing Systems based on Memristive Devices”, Max Plank Institute Seminar, July 2021.

“RRAM based in-memory computing for embedded AI”, The 3rd International Symposium on Memory Devices for Abundant Data Computing, May 2021 (Plenary).

“Scalable Compute-In-Memory Systems Based on Tiled RRAM Fabric”, NSF Workshop on Compute-In-Memory (CIM) Technologies, May 2021.

“Scalable RRAM-based in-memory computing design for embedded AI”, 2021 VLSI-DAT Symposium, April 2021.

“Scalable Neuromorphic and In-Memory Computing Hardware Based on Emerging RRAM Devices,” VLSI SOC symposium, Oct 2020.

“Neuromorphic Computing Based on Memristive Materials and Devices,” European Training Network on Materials for Neuromorphic computing, Oct 2020

“Neuromorphic Computing Based on Memristive Materials and Devices,” Harvard University, Sept 2020

“Temporal data analysis in memristor-based RC systems,” International Conference on Neuromorphic Systems 2020 (ICONS), Oak Ridge National Lab, July 2020

“Scalable Neuromorphic Computing Hardware Based on Emerging RRAM Devices,” Sandia National Lab, June 2020

“Modular RRAM based in-memory computing design for embedded AI,” DATE (Design, Automation and Test in Europe), Grenoble, France, April 2020

“Memristive devices for neuromorphic computing: from multiply-and-accumulate (MAC) operations to dynamic networks”, 2019 IEEE International workshop on future computing (IWOFC), Hangzhou, China, December 2019. (Keynote)

“Memristor devices for neuromorphic computing: from multiply-and-accumulate (MAC) operations to dynamic networks”, Inaugural Chua Memristor Institute Conference, Wuhan, China, November 2019. (Plenary)

“2D materials in resistive memory and neuromorphic computing system applications”, Nature Conference on 2D Materials: Visions of Future Research and Applications, Xi’an, China, November 2019.

“Neuromorphic computing with memristor devices: from multiply-and-accumulate (MAC) operations to dynamic networks”, Nature Conference on Neuromorphic Computing, Beijing, China, October 2019.

“RRAM fabric for neuromorphic computing applications”, Institute of Microelectronics, Tsinghua University, Beijing China, June 2019.

“2D materials in resistive memory and neuromorphic computing system applications”, Device Research Conference (DRC) 2019, Ann Arbor, June 2019.

“RRAM foundations for neuromorphic and in-memory computing systems”, DATE (Design, Automation and Test in Europe), Florence, Italy, March 2019.

“RRAM/memristor foundations for neuromorphic computing and in-memory processing”, Tutorial on Nanotechnology-Enabled Neuromorphic Electronics, Army Research Labs, MD, November, 2018.

“RRAM fabric for neuromorphic and in-memory computing applications”, Hardware and Algorithms for Learning On-a-chip (HALO) workshop, San Diego, CA, October 2018.

“RRAM Fabric for Neuromorphic Computing Applications”, 1st IBM AI Compute Symposium, IBM, NY, October, 2018.

“RRAM fabric for neuromorphic and in-memory computing applications”, Department Seminar, Rochester Institute of Technology, October, 2018.

“RRAM Fabric for Neuromorphic and Compute-In-Memory Systems”, National Tsinghua University, August, 2018

“RRAM fabric for neuromorphic and in-memory computing applications”, Taiwan Semiconductor Manufacturing Corporation (TSMC), August, 2018

“Neuromorphic computing - from materials to circuits”, NanoKorea 2018, Seoul, Korea, July, 2018.

“Memristors for neuromorphic computing”, International Conference on Memristive Materials, Devices & Systems (MEMRISYS 2017), Beijing, China, July, 2018 (Keynote)

“RRAM Fabric for Neuromorphic and Compute-In-Memory Systems”, Applied Materials, Santa Clara, May, 2018.

“Memristors for memory and neuromorphic computing - from materials to circuits”, Massachusetts Institute of Technology (MIT), Cambridge, April, 2018.

“RRAM fabric for neuromorphic and reconfigurable compute-in-memory systems”, IEEE Custom Integrated Circuits Conference (CICC 2018), San Diego, April 2018.

“Memory and Computing Systems Based on Reconfigurable Materials: Merging Electronics with Ionics”, Waterloo Institute of Nanotechnology seminar, University of Waterloo, November 2017

“Feature Extraction and Image analysis using memristor networks”, Neuro-inspired Computing Workshop, San Diego, October 2017

“Feature Extraction and Image analysis using memristor networks”, The 14th US-Korea Forum

on Nanotechnology, Falls Church, September 2017

“Feature Extraction and Image analysis using RRAM networks”, International Symposium on Memory Devices for Abundant Data Computing, Hong Kong, September 2017 (Plenary)

“Feature Extraction and Image analysis using memristor networks”, 1st International Workshop on Future Computing: Memristive Devices and Systems, Beijing, September 2017

“Device Variations and Their Effects on RRAM Applications”, 24th International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA 2017), Chengdu, July 2017 (Keynote)

“Memristive Devices and Networks for Computing”, Tsinghua University, June 2017

“Memory and Computing Systems Based on Resistive Switching Devices: Merging Electronics with Ionics”, ChinaRRAM, Suzhou, June 2017

“Image Analysis Using Memristor Networks”, MRS Spring Meeting, Phoenix, April 2017

“Memristive Devices for Computing”, International Conference on Memristive Materials, Devices and Systems (Memrisys 2017), Athens, April, 2017 (Plenary)

“Nanoelectronics: Merging Electronics with Ionics”, China Semiconductor Technology International Conference, Shanghai, March 2017

“Memory and Computing Systems Based on Resistive Switching Devices: Merging Electronics with Ionics”, Nanotech Seminar Series, USC, February 2017

“Memory and Computing Systems Based on Resistive Switching Devices: Merging Electronics with Ionics”, C-SPIN Center Seminar, University of Minnesota, December 2016

“Nanoelectronics: Merging Electronics with Ionics”, NANO@Wayne Seminar, Wayne State University, November 2016

“Neuromorphic Computing Based on Resistive Switching Devices”, IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT-2016), Hangzhou, China, October 2016

“Visualization, modeling and control of filament growth in resistive-memories (RRAMs) towards commercial applications”, 7th International Workshop on Characterization and Modeling of Memory Devices, Milan, Italy, September 2016

“Memory and Neuromorphic Computing Applications Based on Resistive Switching Devices”, 15th International Workshop on Cellular Nanoscale Networks and their Applications, Dresden, Germany, August 2016

“Memristor Crossbar for Image Processing and Data Clustering”, IRDS Emerging Research Devices NanoCrossbar Workshop, Santa Clara, July 2016

“Resistive Memory (RRAM) and its applications in efficient memory and Neuromorphic computing architectures”, 53rd Design Automation Conference (DAC 2016), Austin, TX, June 2016

“Memristor networks for neuromorphic and arithmetic computing”, Conference on Emerging Technologies Beyond CMOS, Montreal, Canada, May 2016

“Memristors: from devices to neuromorphic computing applications”, Frontiers in Neuromorphics Workshop, UCLA, April 2016.

“Understanding and Control of Dynamic Ionic Processes during Filament Formation in ReRAM Devices,” International Workshop on Advances in ReRAM: Materials & Interfaces, Crete, Greece, October 2015.

“Emerging resistive memory devices and their applications in efficient data storage and computing architectures,” Peking University, Beijing, September 2015.

“Nanoscale resistive devices: mechanisms and applications,” ChinaNANO2015, Beijing, September 2015.

“Efficient Computing Architectures Enabled by Memristive Devices,” Phillips Research Site, Air Force Research Lab, Albuquerque, August 2015.

“Conductive-Bridge RAM (CBRAM): From Operation Principles to Memory Array Applications,” 15th International Conference on Nanotechnology, IEEE (IEEE Nano), Rome, Italy, July 2015.

“Crossbar RRAM– Enabling A New Era of Storage Innovation,” SEMICON West, San Francisco, July 2015.

“Emerging Resistive memory devices and their applications in efficient data storage and computing systems”, Institute of Physics, Chinese Academy of Sciences, Beijing, July 2015.

“Emerging Memory and Logic Systems Based on Two-Terminal Memristive Devices,” University of Southampton, Southampton, UK, February 2015.

“3D ReRAM with Field Assisted Super-Linear Threshold (FASTTM) Selector Technology”, 20th Asia and South Pacific Design Automation Conference (ASP-DAC 2015), Tokyo, Japan, January 2015.

“Memory and Logic Electronics Based on Nanoscale Resistive Switches (Memristors)”, 224th ECS meeting, Cancun, Mexico, October 2014.

“Computing with Memristors: Beyond the Standard Model”, plenary talk, 4th Memristor and Memristive Systems Symposium, Notre Dame, IN, July 2014

“Two-Terminal Nanoscale Resistive Devices for Memory and Computing Applications”, 9th SINO-US Nano Forum, Tianjin, China, July 2014.

“Nanoscale Memristive Devices for Memory and Computing Applications”, Institute of Microelectronics, Peking University, Beijing, China, July 2014.

“Memristive Devices for Stochastic Computing”, IEEE International Symposium on Circuits and Systems (ISCAS), Melbourne, Australia, June 2014,

“Vertical Nanowire Electrical and Optical Devices Based on a Clean Si/Ge Nanowire Heterojunction System”, MRS Spring Meeting, San Francisco, March 2014.

“RRAM Filament Structure and Growth Dynamics”, China Semiconductor Technology International Conference, CSTIC2014, Shanghai, March 2014.

“Nanoscale Memristive Devices for Memory and Computing Applications”, 224th ECS Meeting, San Francisco, October 2013.

“RRAM Filament Structure and Growth Dynamics”, 3rd imec-Stanford International Workshop on Resistive Memories, Leuven, Belgium, October 2013.

Non-Conventional Memory and Logic based on Emerging Two-Terminal Nanoscale Resistive Devices, 2nd Summer School on the Architecture and Properties of Nanomaterials Based Functional Macro-systems, Beijing, China, July 2013.

“Resistive Memories Based on Amorphous Films”, The 9th IEEE Nanotechnology Full Day Symposium, Santa Clara, May 2013.

“Two-Terminal Nanoscale Resistive Switches for Memory and Computing”, Solid State Seminar, Notre Dame University, South Bend, April 2013.

“Resistive Random Access Memory (RRAM): Materials and Devices”, 2013 IEEE Workshop on Microelectronics and Electron Devices (WMED), Boise, April 2013.

“Two-Terminal Nanoscale Resistive Switches for Computing”, Memristors for Computing (MemCo) Workshop, Frejus, France, November 2012.

“Resistive Memory Based on Amorphous Films”, IEEE Non-Volatile Memory Technology Symposium (NVMTS), Singapore, October 2012.

“Two-terminal Nanoscale Resistive Switches for Memory and Logic Applications”, IBM MRC Workshop: New Computation Paradigms, Zurich, Switzerland, August 2012.

“Self-Rectifying Resistive Memory Devices”, SRC e-Workshop, June 2012.

“Self-Rectifying Resistive Memory Devices”, Nature Conference, Aachen, Germany, June

2012.

“Nanoscale Resistive Memory (Memristor) Based on Amorphous Films”, MRS Spring Meeting, San Francisco, April 2012

“Emerging Memory Materials and Devices”, SRC workshop on Future Materials and Processes for Nanotechnology, Tokyo, Japan, February 2012

“Two-Terminal Nanoscale Switches (Memristors) for Memory and Logic Applications”, ChinaNANO2011, Beijing, September 2011

“A Si-Based Memristive System For Memory And Neuromorphic Applications”, Toshiba Corporate R&D Center, Kawasaki, Japan, January 2011

“Two-Terminal Resistive Switches (Memristors) for Memory and Logic Applications”, 16th Asia and South Pacific Design Automation Conference, ASP-DAC 2011, Yokohama, Japan, January 2011

“Electronics Based on Low-Dimensional Systems: Nanowires and Memristors”, Advanced Material Research Lab, Fudan University, December 2010

“Memristor devices and circuits based on oxides”, 3rd International Workshop on Functional Oxides and Applications, Ningbo Institute of Material Technology and Engineering, Chinese Academy of Sciences, December 2010.

“A Si-based memristive system for nanoelectronics applications”, Institute of Microelectronics, Chinese Academy of Sciences, December 2010

“Si Memristive Devices Applied to Memory and Neuromorphic Circuits”, The IEEE International Symposium on Circuits and Systems (ISCAS 2010), Paris, June 2010.

“Nanowire Devices and Circuits”, Liquid Crystal Institute, Kent State University, April 2010.

“Nanowire Based Electronics: Challenges and Prospects”, the International Electronic Device Meeting (IEDM), December 2009.

“Nanoscale Memristive Devices for Memory and Logic Applications”, Condensed Matter Physics seminar, Case Western Reserve University, October 2009.

“Nanowire-Based Thin-film Devices as High-Performance Transparent and Flexible Electronics”, Nanoscale One-Dimensional Electronic and Photonic Devices symposium, Vienna, October 2009.

“Nanoscale memristive devices for memory and logic applications”, Ningbo Institute of Materials Technology and Engineering, Chinese Academy of Sciences, August 2009.

“Nano Devices Based on One-Dimensional Wires”, Institute of Physics, Chinese Academy of Sciences, August 2009.

“Nano-Devices based on One-Dimensional Wires”, IEEE Nanotechnology Technology Council, Southeast Michigan Chapter, May 2009.

“A Si-based memristive system for nanoelectronics application”, Condensed Matter Physics Seminar, Stony Brook University, May 2009.

“Nanoscale Devices Based on One-Dimensional Wires”, Applied Physics Seminar, University of Michigan, March 2009.

“Device Applications Based on One-dimensional Nanowires”, 1st International Workshop on Functional Oxides and Applications, Ningbo Institute of Material Technology and Engineering, Chinese Academy of Sciences, December 2008.

“What Wonderful Things Small (Nano) Wires Can Do For You: From High-Density Memories To Transparent Electronics”, WIMS Seminar, University of Michigan, November 2008.

“The Principle and Applications of Radio-Frequency Single-Electron Transistors”, Center of Quantum Information Seminar, University of Science and Technology of China, October 2008.

“A Si-Based Two-Terminal Resistive Switch For Memory And Neuromorphic Computing Applications”, ECE Department Seminar, Michigan State University, October 2008.

“Nanowire Devices and Their Applications to Displays”, Society for Information Display, 15th

Annual Symposium on Vehicle Displays, Dearborn, October 2008.

“Si-Based Two-Terminal Resistive Switching Nonvolatile Memory”, IEEE-ICSICT, The 9th International Conference on Solid-State and Integrated-Circuit Technology, Beijing, October 2008.

“Properties and Applications of Carbon Nanotubes and Other 1D Nanostructures”, Tutorial, Third International Conference on Nano-Networks, Boston, September 2008.

“More Moore and More Than Moore – A Few Approaches to Nanoelectronics”, Condensed Matter Physics Seminar, Tsinghua University, June 2008.

“Ultra-High Density Silicon-Based Crossbar Memory”, Sandisk Corp., Milpitas, CA, January 2008.

“Nanoelectronic Devices”, Micro/Nano Fabrication Workshop, Ann Arbor, October 2007.

“Nanowires for Nanoscience and Nanotechnology”, plenary talk, IEEE Nano2006, Cincinnati, July 2006.

“Semiconductor Nanowires” Applied Physics Seminar, University of Michigan, Ann Arbor, March 2006.

“One-Dimensional Nanowire Heterostructures”, NERS Colloquium, University of Michigan, Ann Arbor, October 2005.

“One-Dimensional Transport in Semiconductor Nanowires”, WIMS Seminar, University of Michigan, Ann Arbor, October 2005.

“One-Dimensional Transport in Nanowire Heterostructures”, Rowland Institute, Harvard University, Cambridge, July 2005.

“One-Dimensional Transport in Semiconductor Nanowires”, AVS Spring Symposium, Michigan Chapter, East Lansing, May 2005.

“Real-time electron counting studies on charge fluctuations in a semiconductor quantum dot”, SPIE, Austin, May 2005.

“One-Dimensional Transport in Nanowire Heterostructures”, Nanotechnology Seminar Series, Purdue University, West Lafayette, April 2005.

“One-Dimensional Transport in Semiconductor Nanowires”, Physics Seminar, University of California – Los Angeles, Los Angeles, March 2005.

“High-Performance Semiconductor Nanowire Devices”, Intel Corp. Hillsboro, March 2005.

“One-Dimensional Transport in Semiconductor Nanowires”, Condensed Matter Seminar, University of California - Berkeley, Berkeley, March 2005.

“One-Dimensional Transport in Semiconductor Nanowires”, Condensed Matter Seminar, University of Texas - Austin, Austin, February 2005.

“One-Dimensional Transport in Semiconductor Nanowires”, Condensed Matter Seminar, University of California – San Diego, San Diego, January 2005.

US and International Patents (22 issued)
