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Letter

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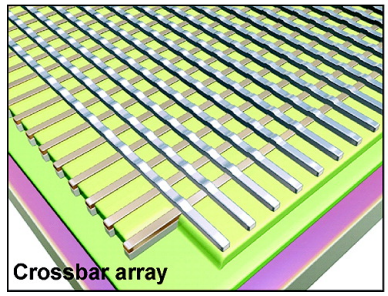

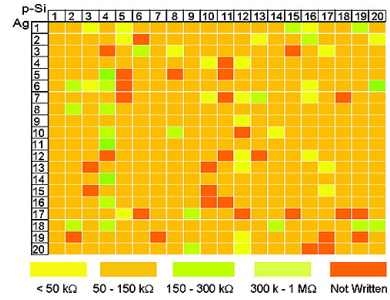

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High-Density Crossbar Arrays Based on a Si Memristive System

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ABSTRACT

We demonstrate large-scale (1 kb) high-density crossbar arrays using a Si-based memristive system. A two-terminal hysteretic resistive switch (memristive device) is formed at each crosspoint of the array and can be addressed with high yield and ON/OFF ratio. The crossbar array can be implemented as either a resistive random-access-memory (RRAM) or a write-once type memory depending on the device configuration. The demonstration of large-scale crossbar arrays with excellent reproducibility and reliability also facilitates further studies on hybrid nano/CMOS systems.

A hysteretic resistive switch consists of a switching medium sandwiched between two electrodes (Figure 1) and exhibits nonlinear $I-V$ characteristics so that the resistance of the device depends not only on the present voltage (or current) value but also the history of the device programming (Figure 1a). The hysteretic resistive switches fall in the category of broadly defined memristive system,[1−3] which has attracted significant interest recently as a promising candidate for future high-density, high-performance memory or logic applications.[1−6] The hysteretic resistive switch-based memristive system offers excellent scaling potential since its simple structure means that only one dimension (the distance between the two electrodes) needs to be critically controlled. Furthermore, a 2D array of such resistive switches can be readily implemented into the so-called crossbar structure by overlaying two nanowire electrode arrays with 90° angle to each other so that a two-terminal switch is formed at each crosspoint[4−8] (Figure 1b). The crossbar structure possesses many attractive features as it offers the highest possible device density and the simplest interconnect configuration that still allows external access to each nanodevice.[4,5,7] In addition, hybrid nanocrossbar/CMOS architectures have been proposed to maximize the advantages provided by the crossbar structure by compensating the limited functionality of two-terminal switches with CMOS components.[8−10] It has been shown that hybrid crossbar/CMOS memories using such approaches can offer terabit potential and sub-100 ns access time. In addition, hybrid logic circuits based on the crossbar/CMOS structures can offer function density of at least 2 orders of magnitude higher than that of their CMOS counterparts fabricated with the same design rules, at the same power density and comparable logic delay.[8−10]

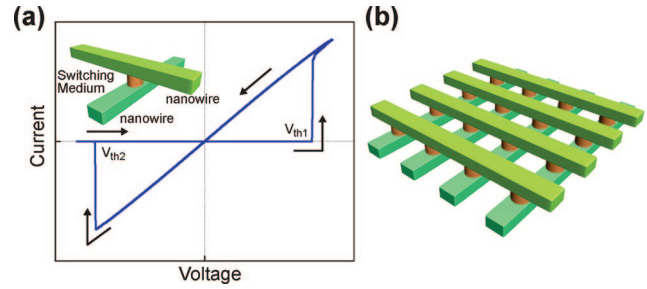

Figure 1. (a) A hysteretic resistive switch (memristive device). Different resistances (ON or OFF) can be obtained at the same voltage depending on whether the programming voltage has passed the write threshold voltage (V_{th1}) or erase threshold voltage (V_{th2}) in the previous operation cycle. Inset, a two-terminal switch can be formed with a switching medium sandwiched between a pair of electrodes. (b) Schematic of a crossbar array formed by the two-terminal switches and nanowire electrodes.

Research on two-terminal resistive switches has so far been focused on binary oxides, ionic conductors, or molecules.[11−15] However, these materials suffer from stability and compatibility issues with CMOS processing. For example, molecular switches offer excellent scaling potential, but have been limited to low yield, low ON/OFF ratio, and slow programming speed.[11,15] Using a solid-state amorphous-Si (a-Si) heterostructure as the switching medium, we and other groups have shown recently that two-terminal resistive switches composed of metal (typically Ag) top electrodes and p-type silicon (p-Si) bottom electrodes are CMOS compatible and offer promising switching characteristics[16−18] in terms of write speed (<10 ns), endurance (>10^5 cycles), retention (~ 7 years), and scaling potential (<30 nm). In this letter,

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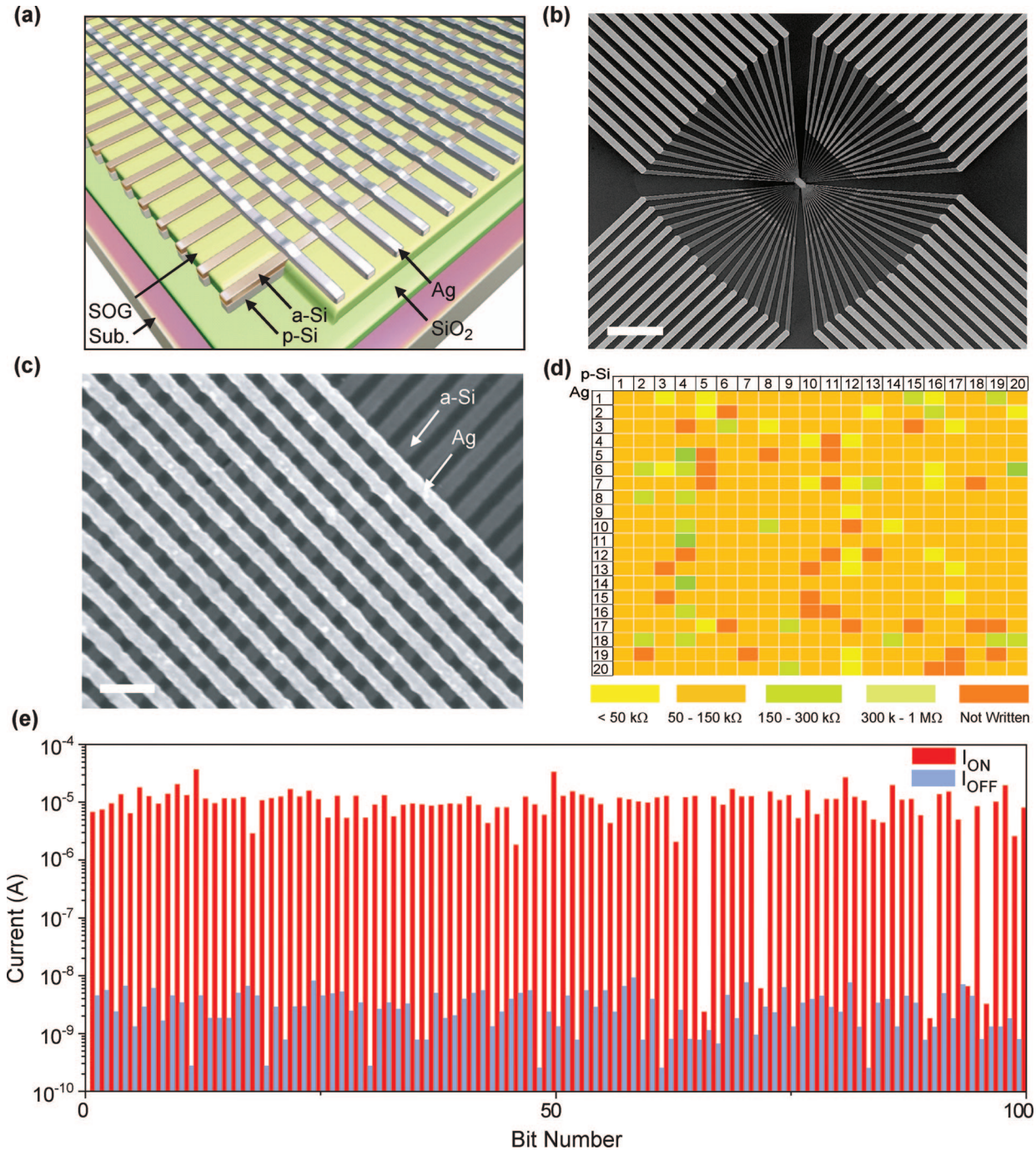

Figure 2. (a) A crossbar array formed with Ag and p-Si nanowire electrodes and a-Si as the active layer. (b) SEM image of a 1 kb array showing the intermediate electrodes. Scale bar: 40 μm. (c) Zoomed-in image of the array in panel b. Scale bar: 200 nm. (d) The yield map of 400 crosspoints within the 1 kb array. Columns and rows correspond to the p-Si and Ag nanowire electrodes, respectively. If a crosspoint was not programmed with 200 μS at 5.5 V pulse, the crosspoint was considered to be "not written". Different colors in the map represent different ON-state resistances of the crosspoints, as explained in the legend. (e) I_{ON} and I_{OFF} of the first 100 bits within the 1 kb array, illustrating the uniformity of the array. ON/OFF ratio $>10^3$ for all devices that are considered written.

we demonstrate large-scale (1 kb), high-density crossbar arrays based on the a-Si memristive system and show that the nanocrossbar arrays exhibit excellent yield, ON/OFF and uniformity. This demonstration, along with success already achieved at the single-cell level, suggests that the a-Si memristive system is well positioned to implement the proposed hybrid crossbar/CMOS systems for ultrahigh performance memory and logic applications.

The crossbar array in our study consists of a parallel array of boron-doped poly silicon nanowires serving as the bottom electrodes, the a-Si active layer, and a parallel array of Ag nanowires serving as the top electrodes as shown in Figure 2. Spin-on-glass (SOG) was used as a dielectric to isolate the top and bottom electrode arrays outside the crosspoints. Detailed discussion on device fabrication can be found in the Supporting Information. Essentially, each crosspoint in

the array forms a two-terminal Ag/a-Si/p-Si switch discussed earlier. Figure 2b,c shows the SEM image of a 1 kb (32 × 32) crossbar array with density of 2 Gbits/cm^2 and line width of 120 nm. Compared with memristive systems based on molecules or metal oxides, using the solid-state a-Si as the switching medium allows high-yield fabrication and operation. For example, the fabrication yield of the 1 kb crossbar array is 98% and each bit inside the 1 kb array can be addressed automatically with high fidelity using a group of preset write/erase/read programming pulses without having to adjust the programming signals manually or knowing the state of the crosspoints. Figure 2d shows the yield map of 400 bits tested using the automated program. The bits were written with 200 μS pulses at 5.5 V. The device parametric yield (defined as the percentage of devices showing ON/OFF ratio $>10^3$ after the write/erase pulses) was 92% with most (80%) devices showing ON resistance in the range of 50−150 kΩ. Figure 2e shows I_{ON} and I_{OFF} values obtained from the first 100 bits within the array, once again demonstrating the high-yield and excellent uniformity of the still unoptimized crossbar array. To our best knowledge, this is the first demonstration of a large scale (kb level or higher) high density crossbar array based on two-terminal hysteretic resistive switches (memristive systems) with high yield, ON/OFF ratio and uniformity.

A relatively large line width of 120 nm was used in the 1 kb array for the bottom p-Si nanowire electrodes to minimize series-resistance associated with the relatively resistive p-Si nanowire electrodes. Even so the resistance associated with the p-Si nanowire electrodes can be up to 30 kΩ that limits fully automated operations of the array. Future improvements will involve the addition of a metal or a silicide layer adjacent to the p-Si layer to reduce the series resistance. The incorporation of the metal layer will in turn allow the use of narrower nanowire electrodes hence resulting in even higher bit density. We note that cell size <50 nm × 50 nm has already been demonstrated at the single-cell level corresponding to a density of 10 Gb/cm^2 limited only by the available lithography technique.[16,17] To demonstrate the feasibility of the crossbar array as high density memory for information storage, a smaller array was tested to mitigate the series resistance effect at this development stage. Figure 3a shows the SEM image of a 16 × 16 crossbar memory with a density of 1.1 Gbits/cm^2 so that larger interconnect electrodes are <8 μm away from each crosspoint to limit the series resistance to <15 kΩ. Figure 3b shows that a word "CrossBar" can be stored and retrieved from 64 bits (an 8 × 8 array) within the crossbar using a fully automated write/read program, where each letter in the word "CrossBar" is represented by an 8-bit ASCII character and written into a single row inside the array.

Crossbar arrays without the p-Si layer have also been studied to verify the role of the p-Si electrode played in the switching process. Figure 4a shows the SEM image of a 1 kb crossbar memory composed with Ag/a-Si/Ni crosspoints. Unlike the Ag/a-Si/p-Si structures in which the ON-resistance can be adjusted by tuning the a-Si growth parameters (e.g., R_{ON} can be controllably varied from the order of 100 MΩ

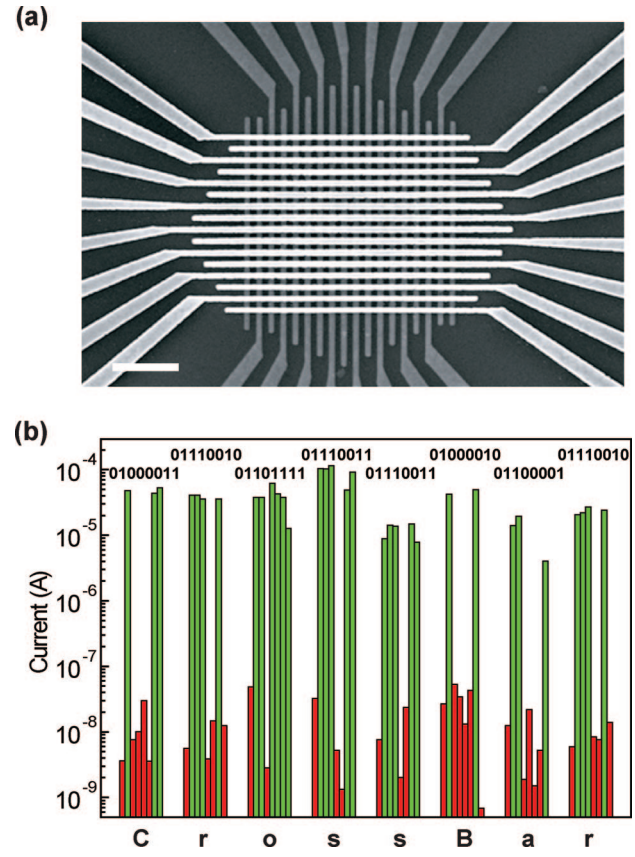

Figure 3. (a) SEM image of a smaller 16 × 16 array. Scale bar: 2 μm. (b) The output from the array showing the word "CrossBar". Each letter is represented by an 8-bit ASCII character shown in the figure.

to 10 kΩ, by adjusting the deposition temperature, Figure 5a), all Ag/a-Si/Ni devices tested have shown low R_{ON} on the order of 1 kΩ and high programming currents on the order of 1 mA hence undesirably large write energy regardless of the a-Si deposition conditions. In addition, the endurance of the Ag/a-Si/Ni devices is typically only a few hundred cycles, much less than the $>10^5$ cycles typically obtained on the Ag/a-Si/p-Si devices,[16,17] possibly due to the stress to the material asserted by the high programming current. We note however that the Ag/a-Si/Ni devices may be suitable as read-only memories (ROMs) or write-once read-many memories since they show excellent retention after the initial programming process (Supporting Information).

The different behaviors in the Ag/a-Si/p-Si devices and Ag/a-Si/Ni devices can be qualitatively understood by examining the mechanism of the resistance switching process. Resistance switching in the a-Si devices has been explained by the formation of conductive filaments inside the a-Si matrix. The filament has been suggested to be in the form of a series of Ag particles[18−21] (Supporting Information). The resistance in ON state is then dominated by the tunneling resistance between the last Ag particle in the filament and the bottom electrode. When the filament grew by a step length as a new Ag particle hops into a new trapping site, the resistance (current) decreases (increases) exponentially, consistent with the experimental observations where stepwise increase in current is observed during the

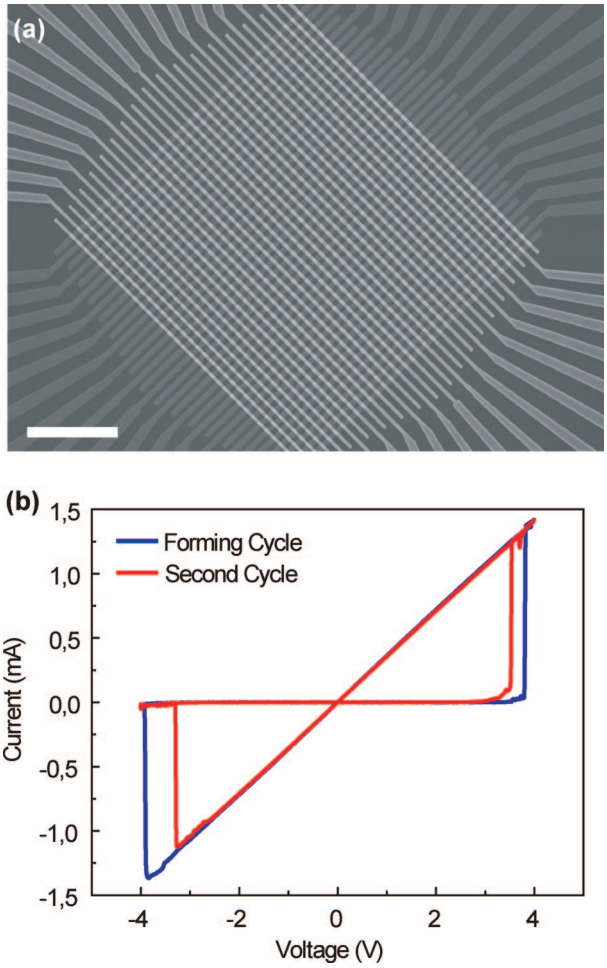

Figure 4. (a) SEM image of a 1 kb crossbar array based on the Ag/a-Si/Ni device structure. Scale bar: 2 μm. (b) Resistance switching characteristics of a typical Ag/a-Si/Ni device inside the array. The initial forming cycle is shown in blue and subsequent cycle is shown in red.

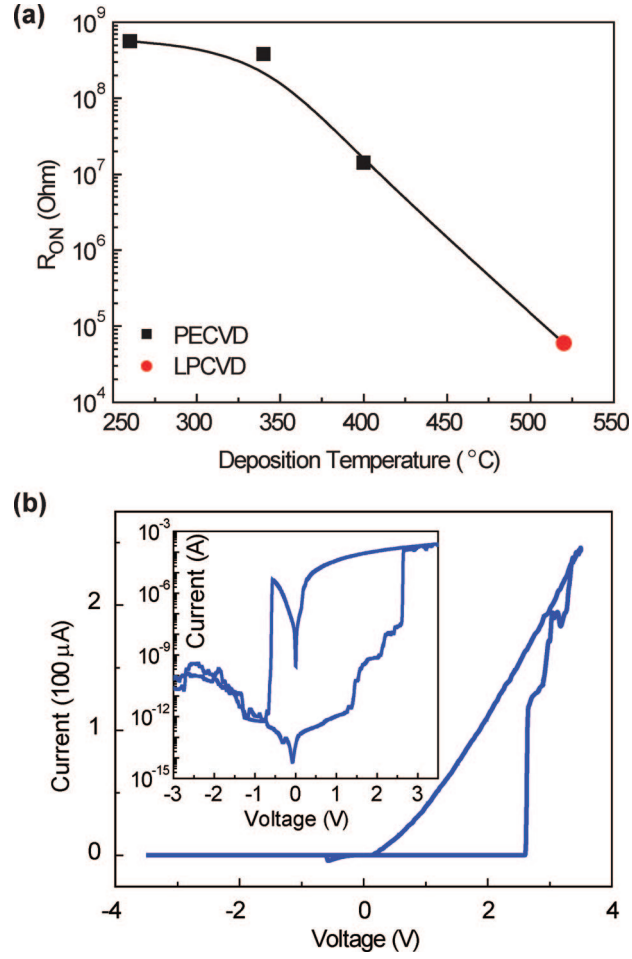

Figure 5. (a) Dependence of R_{ON} on the a-Si deposition condition for the Ag/a-Si/p-Si devices. (b) DC resistance switching characteristics for a typical Ag/a-Si/p-Si device with a 30 nm thick a-Si layer. Inset shows the same $I-V$ curve in semilog plot. Discrete current jumps can be observed at $V \sim 1.5$, 2.1 and 2.6 V.

DC turn-on process (Figure 5b, inset). The change in current can then be calculated[22] to first order within the WKB approximation and is related to the increase in filament length Δd

$$\frac{J(\text{after jump})}{J(\text{before jump})} = e^{-(\sqrt{2m^*\Delta E}/\hbar)2\Delta d} \quad (1)$$

where $J \propto T(\Delta E) \propto e^{-(2/\hbar)\int_0^d (2m^*\Delta E dx)^{1/2}} \propto e^{-(2(2m^*\Delta E)^{1/2}/\hbar)d}$ is the tunneling current density, $T(\Delta E)$ is the tunneling rate, ΔE is the barrier height seen by the electrons, d is the distance between the last Ag particle and the bottom electrode and decreases by Δd after the jump. The barrier height can be estimated to first order to be $\Delta E = \phi_{Ag} - \chi_{Si} = 4.26 - 3.95 = 0.31$ eV and $m^* = 0.09\ m_0$ where m_0 is the free electron mass.[23,24] From eq 1 we can estimate $\Delta d = 2.98$, 1.98, 4.25 nm for the first, second, and third jumps in Figure 5b, respectively. The total filament length can then be calculated to be 9.21 nm. It is worth noting that the estimated chain length is shorter than the a-Si layer thickness of 30 nm, suggesting that a large portion of the conduction path near the top electrode may be formed by large volumes of Ag particles likely formed during the initial forming process,[19,25] while the last ~10 nm section close to the bottom electrode is dominated by a single chain of Ag particles that determine the final ON-state resistance and current of the switch. Studies on other Ag/a-Si/p-Si devices with a-Si thickness of 30 and 60 nm (Supporting Information) show similar estimated filament length of ~10 nm and independent of the physical a-Si layer thickness, further confirming this hypothesis. The dominant role played by the interface region of the a-Si/bottom-electrode can then be used to explain the low R_{ON} observed in Ag/a-Si/Ni devices since a higher concentration of trapping sites for Ag is expected near the a-Si/metal interface compared with the a-Si/p-Si interface, leading to the formation of multiple filaments (or filaments with closely spaced Ag trapping sites) resulting in low R_{ON} in the Ag/a-Si/Ni devices. This hypothesis is also consistent with our earlier observations[16−18] and consistent with the fact that current compliance was needed during the forming process for metal/a-Si/metal devices in earlier studies to prevent device damage due to excess current.[19,20]

In summary, we demonstrated high density crossbar arrays using a nanoscale a-Si-based memristive system. The excellent yield and performance illustrated by this CMOS compatible approach opens the door for further development and testing of novel electrical circuits based on memristive systems. For example, our recent studies on time- and bias-dependent switching characteristics[16] suggest that these

devices may be suitable as synapses in solid-state neuromorphic circuits. Additional improvements of the devices may include incorporating metallic electrodes adjacent to the p-Si nanowire electrodes to mitigate series-resistance problem, and incorporating an n-Si layer adjacent to the p-Si electrode to create a PN diode at each crosspoint to mitigate crosstalk problem. Looking into the future, we expect relatively smooth integration of the a-Si-based crossbar arrays with CMOS components that can lead to a number of high performance hybrid crossbar/CMOS memory and logic systems.

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Supporting Information Available: Fabrication and electrical characterization of the crossbar arrays. Additional discussion on the filament length. This material is available free of charge via the Internet at http://pubs.acs.org.

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