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<b>Interests</b>	Seeking an Internship in Low Power Computer Architecture, System-level Power Management, High Performance Clocking	
<b>Education</b>	<b>University of Michigan, Ann Arbor</b> PhD Candidate, Electrical Engineering and Computer Science (GPA: 7.33/9.00, expected graduation date: May 2010)	Fall 2004 - present
	<b>Indian Institute of Technology, Bombay, India</b> B.Tech and M.Tech, Electrical Engineering (GPA: 9.2/10.0)	1999 - 2004
<b>Research</b>	<b>Power Management for Multicore Systems</b> (Research Assistant, Prof. Kang Shin, Univ. of Michigan, EECS)	2006 – present
	My current research involves system-level design and analytical modeling to improve energy efficiency in data-centers. I have worked on efficient power supply design and memory power saving techniques.	
	<b>Low Power Circuit Design with Energy Recovery Techniques</b> (Research Assistant, Univ. of Michigan)	
	My previous research in circuit design involved the use of resonant power clocks for reducing power consumption. The work involved circuit level design of a Hadamard transform module using Boost Logic and chip design in 0.13 $\mu$ m IBM technology.	2005-2006
	<b>System Reliability and Microarchitecture Design</b>	
	I have also worked on system level reliability and verification, to design and implement a fault tolerant processor with minimal area and power overhead.	2005
<b>Relevant Coursework</b>	Advanced High Performance VLSI Design (EECS 628), VLSI Design II (EECS 627), VLSI Design I (EECS 427), Digital Integrated Technology (EECS 523), Hardware Testing (EECS 579), Computer Architecture, VLSI CAD, Linear Programming (IOE 510), Probability (EECS 401).	
<b>Industry Experience</b>	<b>Intern at Advanced Micro Devices (AMD), Boston, MA.</b> Worked in the high performance clocking group. Designed variable insertion delay and clock duty cycle correction circuits in 45nm SoI technology. Worked on skew, duty cycle and power analysis in the clock grid.	Fall 2006
	<b>Intern at Centre for Artificial Intelligence and Robotics, India.</b> Worked on signal processing. Implemented a custom Isolated word Speech Recognition Algorithm in C and ported it to the TI 6711 DSP. A novel start detection scheme implemented.	Summer 2002
	<b>Intern at Infineon Technologies, Bangalore, India.</b> Worked on the wireless mobile communications. Implemented a full rate channel Codec and implemented it on the Infineon Carmel DSP.	Summer 2001

<b>Publications</b>	“Ultra Low-Cost Defect Protection for Microprocessor Pipelines”, Proc. of the XII International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS).	2006
	“VOLTaiRE: Low-cost Fault Detection Solutions for VLIW Microprocessors”, to be published in the proceedings of Workshop on Introspective Architecture (WISA).	2006
	“On Design and Implementation of an Embedded Automatic Speech Recognition System”, IEEE International Conference on VLSI Design.	2004
<b>Computer skills</b>	VLSI: Mentor graphics, Synopsys and Cadence CAD tools, HSPICE, Nanosim, Verilog. Software: C, Java, Perl, Tcl/Tk. Platform: Intel x86, TI 6x and 2x families, AD Blackfin.	
<b>Projects</b>	Design of a VLIW Alpha processor with on-chip testers in TSMC 0.18 $\mu$ m CMOS technology and a cycle accurate simulator in C.	2005
	Design of a JPEG decoder in 0.25 $\mu$ m CMOS technology with a custom datapath, Huffman decoder, run length decoder and a Booth Multiplier.	2004
	Micro-architectural design of a reconfigurable IP route lookup engine in 0.25 $\mu$ m CMOS technology.	2004
	Design and implementation of a speech recognition system on a custom DSP board around the TI 2407 DSP with a FM wireless link.	2003
<b>Awards</b>	<b>Departmental Fellowship, University of Michigan, Ann Arbor</b>	<b>2004</b>
	1 <sup>st</sup> prize, Electronic Design Project, TechFest, IIT Bombay	2003
	2 <sup>nd</sup> prize, Endeavour, Technological Festival, IIT Kanpur	2003
	3 <sup>rd</sup> prize, Technical Exposition Contest, IIT Bombay	2000
	478 <sup>th</sup> rank (from 150,000 students) in the IIT JEE exam	1999
	20 <sup>th</sup> Merit Rank (from 1.5 million students), State level Matriculation Exam	1996
	17 <sup>th</sup> Merit Rank, Maharashtra State Talent Search Exam	1993
<b>Professional Affiliation</b>	Institute of Electrical and Electronics Engineers (IEEE) student member. Gigascale Systems Research Centre (GSRC).	

References available upon request.