

Variable Delay Gate Design and Clock Grid Simulation

A concise report of the internship at AMD, Boston, 2006.

Sujay Phadke
Univ. of Michigan, Ann arbor

I was working at a co-op engineer at AMD's Boston Design Center. I was part of the clocking group for a microprocessor that the company expects to tape out later this year.

As part of my internship, I was assigned to work on 2 related projects. The first was related to design and optimization of *variable delay circuits*. This module was an essential part of the processor clock tree, in which each of the rising or falling edges of the main system clock could be independently controlled, and a variable delay could be inserted in the clock propagation path. The module required to have minimum introduced clock jitter, low area and power overhead and a known phase relationship between the input and output clock edges.

My first task was to investigate the different circuits in the available literature and elaborate on the pros and cons for each. The use of active control, feedback related topologies was ruled out because of design constraints which could not be met at the given frequencies. I simulated circuits which introduced variable delay using:

- Variable capacitance
- Variable number of stages
- Variable resistance
- Variable drive strength

We settled down on using variable drive strength circuits, which essentially consisted on a novel design based on differential tunable CMOS buffers. The edge rate control was achieved by having a plurality of transistor stacks, each controlled independently with select signals. The operating voltage, transistor threshold voltage, device sizes were all variable. Depending on the drive strength of the stacks and the number of stacks being ON, the edge rate of the output signal was varied over a range of 20ps-100ps. By performing a large set of simulations at various process corners and operating parameters, the optimal numbers for the various components of the circuit were obtained. The circuit helped achieve a good dynamic range for tuning compared to the other circuits, minimal introduced jitter, independent control of both rise and fall edges. (the other circuits that were simulated included: variable capacitance lines, mirror delay line, variable delay using serpentine traces).

The other project that I worked on was concerning repeater and scan clock metal grid. In the processor cores, the various flip-flops can operate either in normal mode, or in scan mode. The scan clock is distributed as a metal grid sandwiched between the power lines, in metals 8 and 9, or 10 and 11. For this experiment, the loading at various points across the grid was estimated and lumped together. The scan clock grid was driven by a tree of tapered buffer stages. The aim was to find out the optimal length, width, spacing of the various sections of the metal grid for the different layers, and obtain the worst case skew, power and area numbers. For this purpose, I designed the circuit and simulated by sweeping the various parameters, to fit the specs closely. The simulation consisted of approx. 50,000 points at different VDD, V_t , metal dimensions, and temperature. For the buffer stages, we tweaked the number of stages, size of the drivers to achieve the required bounds on skew, edge rate and duty cycle corruption.

Most of the simulations were performed in HSPICE. I also wrote perl scripts for netlist modification, data extraction and filtering.

The internship helped me advance my skills in VLSI circuit design and gave me a good sense of work done in the industry and the soft skills required for working in a team.