Celerity: An Open Source RISC-V Tiered Accelerator Fabric


Christopher Batten†, Ronald G. Dreslinski‡, Ian Galton*, Rajesh K. Gupta*, Patrick P. Mercier*, Mani Srivastava§, Michael B. Taylor*, Zhiru Zhang†

* University of California, San Diego
† Cornell University
‡ University of Michigan
§ University of California, Los Angeles
High-Performance Embedded Computing

• Embedded workloads are *abundant* and *evolving*
  • Video decoding on mobile devices
    • Increasing bitrates, new emerging codecs
  • Machine learning (speech recognition, text prediction, …)
    • Algorithm changes for better accuracy and energy performance
  • Wearable and mobile augmented reality
    • Still new, rapidly changing models and algorithms
  • Real-time computer vision for autonomous vehicles
    • Faster decision making, better image recognition

• We are in the post-Dennard scaling era
  • Cost of energy > Cost of area

• How do we attain extreme energy-efficiency while also maintaining flexibility for evolving workloads?
Celerity: Chip Overview

- TSMC 16nm FFC
- 25mm$^2$ die area (5mm x 5mm)
- ~385 million transistors
- 511 RISC-V cores
  - 5 Linux-capable “Rocket Cores”
  - 496-core mesh tiled array “Manycore”
  - 10-core mesh tiled array “Manycore” (low voltage)
- 1 Binarized Neural Network Specialized Accelerator
- On-chip synthesizable PLLs and DC/DC LDO
  - Developed in-house
- 3 Clock domains
  - 400 MHz – DDR I/O
  - 625 MHz – Rocket core + Specialized accelerator
  - 1.05 GHz – Manycore array
- 672-pin flip chip BGA package
- 9-months from PDK access to tape-out
Celerity Overview

Tiered Accelerator Fabric

Case Study: Mapping Flexible Image Recognition to a Tiered Accelerator Fabric

Meeting Aggressive Time Schedule

Conclusion
Decomposition of Embedded Workloads

- General-purpose computation
- Operating systems, I/O, etc.
- Flexible and energy-efficient
- Exploits coarse- and fine-grain parallelism
- Fixed-function
- Extremely strict energy efficiency requirements
An architectural template that maps embedded workloads onto distinct tiers to maximize energy efficiency while maintaining flexibility.
Tiered Accelerator Fabric

General-purpose computation, control flow and memory management
Flexible exploitation of coarse and fine grain parallelism
Tiered Accelerator Fabric

Fixed-function specialized accelerators for energy efficiency requirements
Mapping Workloads onto Tiers

Flexibility

Energy Efficiency

General-Purpose Tier
General-purpose SPEC-style compute, operating systems, I/O and memory management

Massively Parallel Tier
Exploitation of coarse and fine grain parallelism to achieve better energy efficiency

Specialization Tier
Specialty hardware blocks to meet strict energy efficiency requirements
Celerity: General-Purpose Tier
General-Purpose Tier: RISC-V Rocket Cores

• Role of the General-Purpose Tier
  • General-purpose SPEC-style compute
  • Exception handling
  • Operating system (e.g. TCP/IP Stack)
  • Cached memory hierarchy for all tiers

• In Celerity
  • 5 Rocket Cores, generated from Chisel (https://github.com/freechipsproject/rocket-chip)
    • 5-stage, in-order, scalar processor
    • Double-precision floating point
    • I-Cache: 16KB 4-way assoc.
    • D-Cache: 16KB 4-way assoc.
    • RV64G ISA
  • 0.97 mm² per Rocket core @ 625 MHz
Celerity: Massively Parallel Tier Tier
Massively Parallel Tier: Manycore Array

- Role of the Massively Parallel Tier
  - Flexibility and improved energy efficiency over the general-purpose tier by massively exploiting parallelism

- In *Celerity*
  - 496 low power RISC-V Vanilla-5 cores
    - 5-stage, in-order, scalar cores
      - Fully distributed memory model
      - 4KB instruction memory per tile
      - 4KB data memory per tile
  - RV32IM ISA
  - 16x31 tiled mesh array
  - Open source!
  - 80 Gbps full duplex links between each adjacent tile
  - 0.024mm$^2$ per tile @ 1.05 GHz

Diagram:
- MEM Crossbar
- RISC-V Core
- IMEM
- DMEM
- NOC Router
Manycore Array (Cont.)

- XY-dimension network-on-chip (NoC)
  - Unlimited deadlock-free communication
  - Manycore I/O uses same network
- Remote store programming model
  - Word writes into other tile’s data memory
  - MIMD programming model
    - Fine-grain parallelism through high-speed communication between tiles
- Token-Queue architectural primitive
  - Reserves buffer space in remote core
  - Ensures buffer is filled before accessed
  - Tight producer-consumer synchronization
  - Streaming programming model
    - Producer-consumer parallelism
# Manycore Array (Cont.)

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Normalized Area (32nm)</th>
<th>Area Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Celerity Tile @16nm</strong></td>
<td>0.024 * (32/16)^2 = 0.096 mm^2</td>
<td>1x</td>
</tr>
<tr>
<td><strong>OpenPiton Tile @32nm</strong></td>
<td>1.17 mm^2 [1]</td>
<td>12x</td>
</tr>
<tr>
<td><strong>Raw Tile @180nm</strong></td>
<td>16.0 * (32/180)^2 = 0.506 mm^2</td>
<td>5.25x</td>
</tr>
<tr>
<td><strong>MIAOW GPU Compute Unit Lane @32nm</strong></td>
<td>15.0 / 16 = 0.938 mm^2 [2]</td>
<td>9.75x</td>
</tr>
</tbody>
</table>

![Normalized Physical Threads (ALUops) per Area](image)

---


Celerity: Specialization Tier
Specialization Tier: Binarized Neural Network

• Role of the Specialization Tier
  • Achieves high energy efficiency through specialization

• In *Celerity*
  • Binarized Neural Network (BNN)
    • Energy-efficient convolutional neural network implementation
    • 13.4 MB model size with 9 total layers
      • 1 Fixed-point convolutional layer
      • 6 Binary convolutional layers
      • 2 Dense fully connected layers
    • Batch norm calculations done after each layer
  • 0.356 mm$^2$ @ 625 MHz
Parallel Links Between Tiers

- Off-Chip I/O
  - AXI
  - RoCC
  - RISC-V Rocket Core
  - D-Cache
  - I-Cache

General-Purpose Tier
- AXI
- RoCC
- RISC-V Rocket Core
- D-Cache
- I-Cache

Massively Parallel Tier
- RISC-V Core
- XBAR
- I Mem
- D Mem

Specialization Tier
Celerity Overview

Tiered Accelerator Fabric

Case Study: Mapping Flexible Image Recognition to a Tiered Accelerator Fabric

Meeting Aggressive Time Schedule

Conclusion
Case Study: Mapping Flexible Image Recognition to a Tiered Accelerator Fabric

Three steps to map applications to tiered accelerator fabric:

Step 1. Implement the algorithm using the general-purpose tier

Step 2. Accelerate the algorithm using either the massively parallel tier OR the specialization tier

Step 3. Improve performance by cooperatively using both the specialization AND the massively parallel tier
Step 1: Algorithm to Application

Binarized Neural Networks

- Training usually uses floating point, while inference usually uses lower precision weights and activations (often 8-bit or lower) to reduce implementation complexity
- Rastergari et al. [3] and Courbariaux et al. [4] have recently shown single-bit precision weights and activations can achieve an accuracy of 89.8% on CIFAR-10
- Performance target requires ultra-low latency (batch size of one) and high throughput (60 classifications/second)

Step 1: Algorithm to Application
Characterizing BNN Execution

- Using just the general-purpose tier is 200x slower than performance target
- Binarized convolutional layers consume over 97% of dynamic instruction count
- Perfect acceleration of just the binarized convolutional layers is still 5x slower than performance target
- Perfect acceleration of all layers using the massively parallel tier could meet performance target but with significant energy consumption

<table>
<thead>
<tr>
<th>Execution Time (%)</th>
<th>2.15%</th>
<th>23.11%</th>
<th>12.02%</th>
<th>23.98%</th>
<th>12.85%</th>
<th>25.68%</th>
<th>0.2%</th>
<th>0.02%</th>
<th>&lt;0.01%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Weights’ Size (Mbits)</td>
<td>0.003</td>
<td>0.14</td>
<td>0.28</td>
<td>0.56</td>
<td>1.13</td>
<td>2.25</td>
<td>8</td>
<td>1</td>
<td>0.01</td>
</tr>
<tr>
<td>Input Size (Kbits)</td>
<td>60</td>
<td>128</td>
<td>32</td>
<td>64</td>
<td>16</td>
<td>32</td>
<td>8</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Diagram showing the execution time and size breakdown for different layers.
Step 2: Application to Accelerator

BNN Specialized Accelerator

1. Accelerator is configured to process a layer through RoCC command messages.
2. Memory Unit starts streaming the weights into the accelerator and unpacking the binarized weights into appropriate buffers.
3. Binary convolution compute unit processes input fmaps and weights to produce output fmaps.
Step 2: Application to Accelerator

BNN Specialized Accelerator

1. The accelerator is configured to process a layer through RoCC command messages.
2. The memory unit starts streaming the weights into the accelerator and unpacking the binarized weights into appropriate buffers.
3. The binary convolution compute unit processes input feature maps and weights to produce output feature maps.
Step 2: Application to Accelerator

BNN Specialized Accelerator

1. Accelerator is configured to process a layer through RoCC command messages.
Step 2: Application to Accelerator

**BNN Specialized Accelerator**

1. Accelerator is configured to process a layer through RoCC command messages.

2. Memory Unit starts streaming the weights into the accelerator and unpacking the binarized weights into appropriate buffers.
Step 2: Application to Accelerator

BNN Specialized Accelerator

1. Accelerator is configured to process a layer through RoCC command messages

2. Memory Unit starts streaming the weights into the accelerator and unpacking the binarized weights into appropriate buffers
Step 2: Application to Accelerator

BNN Specialized Accelerator

1. Accelerator is configured to process a layer through RoCC command messages

2. Memory Unit starts streaming the weights into the accelerator and unpacking the binarized weights into appropriate buffers
1. Accelerator is configured to process a layer through RoCC command messages

2. Memory Unit starts streaming the weights into the accelerator and unpacking the binarized weights into appropriate buffers

3. Binary convolution compute unit processes input activations and weights to produce output activations
1. Accelerator is configured to process a layer through RoCC command messages.

2. Memory Unit starts streaming the weights into the accelerator and unpacking the binarized weights into appropriate buffers.

3. Binary convolution compute unit processes input activations and weights to produce output activations.
Step 2: Application to Accelerator

BNN Specialized Accelerator

1. Accelerator is configured to process a layer through RoCC command messages.

2. Memory Unit starts streaming the weights into the accelerator and unpacking the binarized weights into appropriate buffers.

3. Binary convolution compute unit processes input activations and weights to produce output activations.
Step 2: Application to Accelerator Design Methodology

```c
void bnn::dma_req() {
    while (1) {
        DmaMsg msg = dma_req.get();

        for (int i = 0; i < msg.len; i++) {
            HLS_PIPELINE_LOOP( HARD_STALL, 1 );

            int req_type = 0;
            word_t data = 0;
            addr_t addr = msg.base + i * 8;

            if (type == DMA_TYPE_WRITE) {
                data = msg.data;
                req_type = MemReqMsg::WRITE;
            } else {
                req_type = MemReqMsg::READ;
            }

            memreq.put(MemReqMsg(req_type, addr, data));
        }

        dma_resp.put(DMA_REQ_DONE);
    }
}
```
Step 2: Application to Accelerator

Design Methodology

- HLS enabled quick implementation of an accelerator for an emerging algorithm
  - Algorithm to initial accelerator in weeks
  - Rapid design-space exploration

- HLS greatly simplified timing closure
  - Improved clock frequency by 43% in few days
  - Easily mitigated long paths at the interfaces with latency insensitive interfaces and pipeline register insertion

- HLS tools are still evolving
  - Six weeks to debug tool bug with data-dependent access to multi-dimensional arrays
Step 2: Application to Accelerator

General-Purpose Tier for Weight Storage

- The BNN specialized accelerator can use one of the Rocket cores’ caches to load every layer’s weights; but, it is inefficient due to off-chip traffic.

Instead, weights can be stored in the massively parallel tier.

Each core in the massively parallel tier executes a remote load-store program to orchestrate sending weights to the specialization tier via a hardware FIFO.
Step 2: Application to Accelerator

General-Purpose Tier for Weight Storage

- The BNN specialized accelerator can use one of the Rocket cores’ caches to load every layer’s weights; but, it is inefficient due to off-chip traffic.
Step 2: Application to Accelerator

General-Purpose Tier for Weight Storage

- The BNN specialized accelerator can use one of the Rocket cores’ caches to load every layer’s weights; but, it is inefficient due to off-chip traffic.

- A large L2 or more storage in the BNN specialized accelerator could improve performance.
Step 3: Assisting Accelerators

General-Purpose Tier for Weight Storage

- The BNN specialized accelerator can use one of the Rocket cores’ caches to load every layer’s weights; but, it is inefficient due to off-chip traffic.
- A large L2 or more storage in the BNN specialized accelerator could improve performance.
- Instead, weights can be stored in the massively parallel tier.
Step 3: Assisting Accelerators

Massively Parallel Tier for Weight Storage

- The BNN specialized accelerator can use one of the Rocket cores’ caches to load every layer’s weights; but, it is inefficient due to off-chip traffic.
- A large L2 or more storage in the BNN specialized accelerator could improve performance.
- Instead, weights can be stored in the massively parallel tier.
- Each core in the massively parallel tier executes a remote-load-store program to orchestrate sending weights to the specialization tier via a hardware FIFO.
Step 3: Assisting Accelerators
Massively Parallel Tier for Weight Storage

- The BNN specialized accelerator can use one of the Rocket cores’ caches to load every layer’s weights; but, it is inefficient due to off-chip traffic
- A large L2 or more storage in the BNN specialized accelerator could improve performance
- Instead, weights can be stored in the massively parallel tier
- Each core in the massively parallel tier executes a remote-load-store program to orchestrate sending weights to the specialization tier via a hardware FIFO
Step 3: Assisting Accelerators

Massively Parallel Tier for Weight Storage

- The BNN specialized accelerator can use one of the Rocket cores’ caches to load every layer’s weights; but, it is inefficient due to off-chip traffic.
- A large L2 or more storage in the BNN specialized accelerator could improve performance.
- Instead, weights can be stored in the massively parallel tier.
- Each core in the massively parallel tier executes a remote-load-store program to orchestrate sending weights to the specialization tier via a hardware FIFO.
Step 3: Assisting Accelerators
Massively Parallel Tier for Weight Storage

- The BNN specialized accelerator can use one of the Rocket cores’ caches to load every layer’s weights; but, it is inefficient due to off-chip traffic
- A large L2 or more storage in the BNN specialized accelerator could improve performance
- Instead, weights can be stored in the massively parallel tier
- Each core in the massively parallel tier executes a remote-load-store program to orchestrate sending weights to the specialization tier via a hardware FIFO
Step 3: Assisting Accelerators
Massively Parallel Tier for Weight Storage

- The BNN specialized accelerator can use one of the Rocket cores’ caches to load every layer’s weights; but, it is inefficient due to off-chip traffic.

- A large L2 or more storage in the BNN specialized accelerator could improve performance.

- Instead, weights can be stored in the massively parallel tier.

- Each core in the massively parallel tier executes a remote-load-store program to orchestrate sending weights to the specialization tier via a hardware FIFO.
Step 3: Assisting Accelerators

Massively Parallel Tier for Weight Storage

- The BNN specialized accelerator can use one of the Rocket cores’ caches to load every layer’s weights; but, it is inefficient due to off-chip traffic.
- A large L2 or more storage in the BNN specialized accelerator could improve performance.
- Instead, weights can be stored in the massively parallel tier.
- Each core in the massively parallel tier executes a remote-load-store program to orchestrate sending weights to the specialization tier via a hardware FIFO.
Step 3: Assisting Accelerators

Massively Parallel Tier for Weight Storage

- The BNN specialized accelerator can use one of the Rocket cores’ caches to load every layer’s weights; but, it is inefficient due to off-chip traffic.
- A large L2 or more storage in the BNN specialized accelerator could improve performance.
- Instead, weights can be stored in the massively parallel tier.
- Each core in the massively parallel tier executes a remote-load-store program to orchestrate sending weights to the specialization tier via a hardware FIFO.
Step 3: Assisting Accelerators

Massively Parallel Tier for Weight Storage

- The BNN specialized accelerator can use one of the Rocket cores’ caches to load every layer’s weights; but, it is inefficient due to off-chip traffic.

- A large L2 or more storage in the BNN specialized accelerator could improve performance.

- Instead, weights can be stored in the massively parallel tier.

- Each core in the massively parallel tier executes a remote-load-store program to orchestrate sending weights to the specialization tier via a hardware FIFO.
Performance Benefits of Cooperatively Using the Massively Parallel and the Specialization Tiers

<table>
<thead>
<tr>
<th></th>
<th>General-Purpose Tier</th>
<th>Specialization Tier</th>
<th>Specialization + Massively Parallel Tiers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Runtime per Image (ms)</td>
<td>4,024</td>
<td>5.8</td>
<td>3.3</td>
</tr>
<tr>
<td>Speedup</td>
<td>1x</td>
<td>~700x</td>
<td>~1,220x</td>
</tr>
</tbody>
</table>

**General-Purpose Tier**
Software implementation assuming ideal performance estimated with an optimistic one instruction per cycle

**Specialization Tier**
Full-system RTL simulation of the BNN specialized accelerator running with a frequency of 625 MHz

**Specialization + Massively Parallel Tiers**
Full-system RTL simulation of the BNN specialized accelerator with the weights being streamed from the manycore
Tiered Accelerator Fabric

Case Study: Mapping Flexible Image Recognition to a Tiered Accelerator Fabric

Meeting Aggressive Time Schedule

Conclusion
How to make a complex SoC?

• Reuse
  • Open-source and third-party IP
  • Extensible and parameterizable designs

• Modularize
  • Agile design and development
  • Early interface specification

• Automate
  • Abstracted implementation and testing flows
  • Highly automated design
How to make a complex SoC? *in 9 months*

- **Reuse**
  - Open-source and third-party IP
  - Extensible and parameterizable designs

- **Modularize**
  - Agile design and development
  - Early interface specification

- **Automate**
  - Abstracted implementation and testing flows
  - Highly automated design
How to make a complex SoC? in 9 months with grad students

• Reuse
  • Open-source and third-party IP
  • Extensible and parameterizable designs

• Modularize
  • Agile design and development
  • Early interface specification

• Automate
  • Abstracted implementation and testing flows
  • Highly automated design
How to make a complex SoC?

• Reuse
  • Open-source and third-party IP
  • Extensible and parameterizable designs

• Modularize
  • Agile design and development
  • Early interface specification

• Automate
  • Abstracted implementation and testing flows
  • Highly automated design

in 9 months
with grad
students
across 4
locations
How to make a complex SoC?

• Reuse
  • Open-source and third-party IP
  • Extensible and parameterizable designs
• Modularize
  • Agile design and development
  • Early interface specification
• Automate
  • Abstracted implementation and testing flows
  • Highly automated design

in 9 months with grad students across 4 locations in 16nm
How to make a complex SoC?

- **Reuse**
  - Open-source and third-party IP
  - Extensible and parameterizable designs

- **Modularize**
  - Agile design and development
  - Early interface specification

- **Automate**
  - Abstracted implementation and testing flows
  - Highly automated design
Reuse

• Basejump: Open-source polymorphic HW components
  • **Design libraries**: BSG IP Cores, BGA Package, I/O Pad Ring
  • **Test infrastructure**: Double Trouble PCB, Real Trouble PCB
  • Available at [bjump.org](http://bjump.org)

• RISC-V: Open-source ISA
  • **Rocket core**: high performance RV64G in-order core
  • **Vanilla-5**: high efficiency RV32IM in-order core

• RoCC: Open-source on-chip interconnect
  • Common interface to connect all 3 compute tiers

• Extensible designs
  • **BSG Manycore**: fully parameterized RTL and APR scripts

• Third Party IP
  • ARM Standard Cells, I/O cells, RF/SRAM generators
Modularize

• Agile design
  • Hierarchical design to reduce tool time
  • Optimize designs at the component level
  • Black-box designs for use across teams
  • SCRUM-like task management
  • Sprinting to “tape-ins”

• Establish interfaces early
  • Establish design interfaces early (RoCC, Basejump)
  • Use latency-insensitive interfaces to remove cross-module timing dependencies
  • Identify specific deliverables between different teams (esp. analog→digital)
Automate

• Abstract implementation and testing flows
  • Develop implementation flow adaptable to arbitrary designs
  • Use validated IP components to focus only on integration testing
  • Use high-level testing abstractions to speed up test development (PyMTL)

• Automate design using tools
  • Use High-Level Synthesis to speed up design-space exploration and implementation
  • Use digital design flow to create traditionally analog components
Synthesizable PLL

- **Reuse**
  - Interfaces and some components reused from previous designs

- **Modularize**
  - Controlled via SPI-like interface
  - Isolated voltage domain for all 3 PLLs to remove power rail noise

- **Automate**
  - Fully synthesized using digital standard cells
  - Manual placement of ring oscillators, auto-placement of other logic
  - Very easy to create additional DCOs that cover additional frequency ranges

<table>
<thead>
<tr>
<th>Area</th>
<th>0.0059 mm$^2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency range*</td>
<td>20 - 3000 MHz</td>
</tr>
<tr>
<td>Frequency step*</td>
<td>2%</td>
</tr>
<tr>
<td>Period jitter*</td>
<td>2.5 ps</td>
</tr>
</tbody>
</table>

* Collected via SPICE on extracted netlist
Synthesizable LDO

- **Reuse**
  - Taped out and tested in 65nm [5], waiting on 16nm results

- **Automate**
  - Fully synthesized controller
  - Custom power switching transistors
  - Post-silicon tunable

- **Compared to conventional N-bit digital LDOs:**
  - $2^N/N$ times smaller
  - $2^N/N$ times faster
  - $2^N$ times lower power
  - $2^{2N}/N$ better FoM

### Controller Area

- $< 0.0023 \text{ mm}^2$

### Decap Area

- $< 0.0741 \text{ mm}^2$

### Voltage Range

- $0.45 – 0.85 \text{ V}$

### Peak Efficiency

- $> 99.8 \%$

---

Celerity Overview

Tiered Accelerator Fabric

Case Study: Mapping Flexible Image Recognition to a Tiered Accelerator Fabric

Meeting Aggressive Time Schedule

Conclusion
Conclusion

• Tiered accelerator fabric: an architectural template for embedded workloads that enable performance gains and energy savings without sacrificing programmability

• Celerity: a case study for accelerating low-latency, flexible image recognition using a binarized neural network that illustrates the potential for tiered accelerator fabrics

• Reuse, modularization, and automation enabled an academic-only group to tape out a 16nm ASIC with 511 RISC-V cores and a specialized binarized neural network accelerator in only 9 months
Acknowledgements

This work was funded by DARPA under the Circuit Realization At Faster Timescales (CRAFT) program

Special thanks to Dr. Linton Salmon for program support and coordination