Integration of organic insulator and self-assembled gold nanoparticles on Si MOSFET for novel non-volatile memory cells

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Available online 19 March 2004

Abstract

We have fabricated a hybrid non-volatile gold nanoparticle floating-gate memory metal insulator semiconductor field effect transistor (MISFET) device combining silicon technology and organic thin film deposition. The nanoparticles are deposited by chemical processes at room temperature over a 5 nm thermal silicon dioxide layer. A multi-layer organic insulator (cadmium arachidate) deposited by the Langmuir–Blodgett technique at room temperature covers the nanoparticle layer and separates it from an Al gate electrode. Charge injection/rejection into the nanoparticles takes place by applying different voltage pulses (less than ±6 V) to the gate electrode, resulting in significant threshold-voltage shift. Charge retention measurements reveal that the device has non-volatile behavior.

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Keywords: Nanoparticles; Nanocrystal memory; Non-volatile memory; Hybrid silicon-organic memory

1. Introduction

Nanocrystal floating-gate memory devices offer an alternative to floating-gate electrical erasable programmable read only memory (EEPROM) devices with gate stack dielectrics [1]. These devices make use of nanometer-size semiconductor or metallic crystals as charge-storage elements. Charging of the nanocrystals occurs via a tunneling oxide from the device channel by the application of voltage pulses to the gate electrode. This, in turn, results in a threshold-voltage shift of the device. Discharge is accomplished by applying opposite polarity pulses to the gate.

Many techniques have been developed to provide embedded nanocrystals within the gate oxide or on top of a tunneling oxide. Most of the efforts reported focus on either silicon or germanium...
nanocrystal formation using low-energy ion implantation and subsequent annealing [2], aerosol deposition [3] or oxidation of a SiGe layer [4]. Formation of metallic nanoparticles has also been employed [5]. All these techniques use high-temperature processes to form the nanoparticles, and pay attention to complementary metal oxide semiconductor (CMOS) technology compatibility.

Meanwhile, other research groups have reported the influence of molecular films or molecules on current flowing through a reversed geometry silicon field effect transistor (FET) [6] or in silicon nanowires [7]. Molecular films have also been used as insulators in all-organic electronic devices [8] or hybrid devices [9]. In parallel, there is currently an effort to demonstrate memory properties in organic devices [10–12]. Our work combines the above ideas with that of nanocrystal memory to demonstrate a new hybrid device that in the future could realize low-cost hybrid silicon-organic memories or all-organic memories fabricated at room temperature.

2. Experimental procedure

A commercially available p-type separated by implanted oxygen (SIMOX) wafer with silicon over-layer thickness of 200 nm and a buried oxide thickness of 400 nm is used as the starting material. After forming the source and drain (S/D) areas of the device a thermal oxide of 5 nm has been grown followed by the formation of Al contacts to S/D regions. Gate oxide has been fabricated on the SIMOX substrate. After this the wafer was cut into small pieces (2 cm × 2 cm each). Several reference samples are then fabricated: metal oxide semiconductor field effect transistor (MOSFET) devices with Al gate (samples A), metal insulator semiconductor field effect transistor (MISFET) devices with the SiO₂ gate oxide coated with a film of cadmium arachidate organic insulator, 54 nm thick, using the Langmuir–Blodgett (LB) technique [13] and utilizing Al as gate metal (samples B) and finally MISFET devices with the gold nanoparticle layer between the two insulating layers mentioned above (samples C), as shown in Fig. 1.

The gold nanoparticle layer was deposited on the SiO₂ substrates at room temperature and pressure by chemical self-assembled processing. In this process the SiO₂ surface was first functionalized with an amine by placing the wafers into a 10% silane solution (1 ml APTES in 9 ml toluene) ($\text{APTES} = 3$-aminopropyltrimethoxysilane) for 1 h under nitrogen environment, washed in toluene and then sonicated in a fresh toluene solution for 2 min each. This process is repeated twice. The chemical reaction that takes place at the oxide surface covers the SiO₂ layer with an amine compound, leaving a NH₂ functionality exposed. A schematic diagram of the resulting surface is shown in Fig. 2(a). The functionalized substrate is dried with nitrogen and held under running ultra-pure water for about 1–2 min to encourage charging of the amino groups prior to exposure to the nanoparticles. This surface was then dipped into a solution of carboxylic acid (–COOH) derivatised Au nanoparticles. The Au nanoparticles were passivated with organic ligands, as shown in Fig. 2(b) [14,15]. Provided that the pH was adjusted correctly, the acid and amine were mutually attracted. The nanoparticles were therefore positioned at a distance from the SiO₂.
surface equal to the length of the amine plus the acid ‘units’ – probably 5–6 nm.

Cadmium arachidate (CdA) film was used to cap the gold-nanoparticle layer. Twenty CdA layers, corresponding to 54 nm total thickness, were deposited by Langmuir–Blodgett technique using a molecular photonics LB700 trough. Cadmium arachidate films were obtained by spreading arachidic acid (Sigma, 99% purity) on a water subphase containing 2.5 \( \times \) 10\(^{-4}\) M cadmium chloride (BDH, Analar Grade). The film depositions were undertaken at a water subphase pH of 5.8 \( \pm \) 0.2 and a temperature of 20 \( \pm \) 2 °C. The deposition pressure for these fatty acid salt films was 22 mN m\(^{-1}\).

New Al metallization and gate electrode patterning processes have been developed in order to overcome the temperature limitation (lower than 75 °C) for the underlying organic films. The Al was deposited at a thickness of 150 nm by e-gun evaporation at low rates (15 A/s) to prevent sample heating. Since standard photolithography process cannot be used, a new Al etching process was developed which consists of the following steps: AZ5214 photoresist is pre-baked at \( T = 65 \) °C for 60 min. The photoresist is patterned, followed by a post-bake step at 65 °C for 90 min on a hot plate. Aluminum etching is performed by dipping the samples into AZ726 developer for 90 s at room temperature (Fig. 3); etching is attributed to the presence of the tetramethylammonium hydroxide (TMAH) [16] contained at a concentration of 0.26 N in this developer. Finally, the remaining resist is removed using acetone in an ultrasonic bath. It should be noted that for pre-bake temperatures lower than 60 °C the photolithography is not possible.

3. Results and discussion

Transmission electron microscopy and atomic force microscopy are used to reveal the presence of gold nanoparticles of mean diameter 5 nm and density 5 \( \times \) 10\(^{12}\) cm\(^{-2}\). The particles are quite small, uniform and stable, suggesting their use in memory devices.

The transfer characteristics (\( I_{DS}–V_{GS} \)) in the linear region (\( V_{DS} = 100 \) mV) have been compared for the three types of FET devices (A, B, C). A threshold voltage, \( V_{th} \) [17], variation is noted as the insulator stack configuration changes; this is mainly attributed to the presence of fixed charges in the organic insulator, already observed in other LB deposited insulators and explained as trapped charge at the interfaces between sequentially deposited layers [18]. Point defects observed by other researchers in LB deposited cadmium arachidate films could also result in fixed charges [19].

Test and measurements of the memory characteristics of these devices consist into the application of positive or negative voltage pulses...
successively on the gate of a previously unstressed device, keeping source and drain electrodes grounded. The voltage pulse height progressively increases while the preselected pulse duration is kept constant. The injected (rejected) charges into (out of) the gold nanoparticles cause shift of the transistor threshold voltage to higher or lower values compared to the unstressed device. The high \( V_{th} \) state is usually called “write” state and the low \( V_{th} \) state is called “erase” state.

The final device exhibits clear memory window under different gate bias pulses of 1 s duration, as shown in Fig. 4. No significant programming window can be obtained with pulse period below 1 s. Since no hysteresis is observed for a gate-voltage cycle for reference samples without Au nanocrystals (samples A and B) then we conclude that the charge storage is due to them. It is important to be noted that the application of positive pulses to the gate lowers the \( V_{th} \) of an unstressed device indicating that electrons are extracted from the nanoparticles to the gate. The application of negative pulses increases the \( V_{th} \) values due to electron injection from the gate metal into the gold nanoparticles. This mechanism reveals that the transistor channel does not contribute to the charge exchange and hence cannot affect the memory properties of the hybrid device. Although the SiO\(_2\) layer used in this work is relatively thin (5 nm), the distance between the surface of the silicon and the gold particles is effectively increased to over 10–11 nm because of the presence of the amine functionalising layer and the organic ligands associated with the Au nanoparticles. This prevents easy charge transfer via tunneling from the semiconductor (channel) to the Au. In addition, it has been shown that the conduction mechanism of LB insulating films is due to tunnelling hopping conduction between the stacked monolayers [20] and has been shown elsewhere that the 54 nm LB CdA film is more conductive than the SiO\(_2\) insulator [21]. So, the increase of electric field across the gate insulator stack in order to inject charges into the nanoparticles enhances the conduction through the organic insulator.

For checking the non-volatility of these memory devices, charge-retention measurements at room temperature have been performed through application of \( \pm 6 \) V gate voltage stress for 1 s with a source to drain bias at 0.1 V. The device is initially driven to the “write” or the “erase” state applying the proper gate pulse and then gate is grounded. The \( I_{DS} \) current is periodically measured at preselected time intervals. For this purpose at these moments a fixed gate voltage, \( V_{read} \), is applied. Current increase or decrease is due to the charge loss for the write or the erase state to the unstressed one. Charge retention measurements shown in Fig. 5 reveal that the memory window does not practically change up to \( 4 \times 10^4 \) s. However, the endurance of the tested MISFET memory structures does not exceed a hundred write/erase cycles. This is most likely due to the degradation of the organic insulator because of the flow of charging the nanoparticles current. To observe charging from the channel that is expected to

![Fig. 4. Write/erase memory window after application of gate voltage pulses with 1 s duration.](image)

![Fig. 5. Charge retention characteristics of the demonstrated memory device.](image)
substantially increase the endurance cycles, the organic insulator will be replaced in future work with a less conductive insulator.

4. Conclusions

We have shown that gold nanoparticles of 5 nm mean size can be self-assembled on the surface of the gate oxide of a conventional FET by following a simple surface functionalization process. Completion of the device includes the deposition of an LB deposited organic insulator that separates the nanoparticle layer from the Al metal gate. The devices exhibit non-volatile memory characteristics at low operation voltages (<± 6 V), are batch fabricated, and their characteristics are stable with time in normal ambient conditions. This technology has also the potential to be explored for application in organic memory devices.

Acknowledgements

The authors acknowledge the financial support from EC through the FET-IST project FRAC-TURE (contract number: 26014).

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