

Lauren Biernacki

PH.D. CANDIDATE · COMPUTER SCIENCE AND ENGINEERING

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Biography

Interested in developing secure and confidential computing systems by strengthening what underlies all machines—the hardware layer. Graduate level research has focused on thwarting memory manipulation and control flow attacks, and maintaining the confidentiality of private data through compiler-level and architectural modifications to general-purpose processors. Passionate about research, teaching, and spreading the joys of computer science with the younger generation.

Education

University of Michigan

Ann Arbor, MI

PH.D. IN COMPUTER SCIENCE AND ENGINEERING, *GPA: 4.0/4.0*

Sept. 2017—PRESENT

- *Advisor:* Prof. Todd Austin, *Concentration:* Computer Architecture & Security

M.S.E. IN COMPUTER SCIENCE AND ENGINEERING, *GPA: 4.0/4.0*

Sept. 2017—May 2019

- *Selected Coursework:* Advanced Topics in Computer Architecture, Computer and Network Security, Advanced Compilers

University of Connecticut

Storrs, CT

B.S.E. IN COMPUTER SCIENCE AND ENGINEERING, *GPA: 3.95/4.0*

Sept. 2013 - May 2017

- Mathematics Minor | Summa Cum Laude, Honors Scholar

Awards & Honors

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| 2017 | Rackham Merit Ph.D. Fellowship , University of Michigan Graduate School
<i>Full funding for two years; Awarded to PhD students with outstanding academic background</i> | Ann Arbor, MI |
| 2017 | School of Engineering Student Commencement Speaker , University of Connecticut
<i>Nominated and selected by School of Engineering faculty as the sole student speaker</i> | Storrs, CT |
| 2017 | Honors Scholar , University of Connecticut
<i>Awarded to students upon completion of the Honors Scholar Program</i> | Storrs, CT |
| 2017 | Outstanding Senior Women Academic Achievement , University of Connecticut
<i>Sole awardee from the School of Engineering out of all graduating seniors</i> | Storrs, CT |
| 2017 | 1st Place Computer Science and Engineering Senior Design , University of Connecticut
<i>Best project out of 26 teams; Awarded by a panel of faculty and industry judges</i>
<i>Title: “Distributed Computing on the Blockchain: Electronic Pollbooks over the Ethereum”</i> | Storrs, CT |
| 2013 | Presidential Scholarship , University of Connecticut
<i>Full-tuition funding for four years; Awarded to high school seniors ranked first in their graduating class</i> | Storrs, CT |

Publications

Under Review

1. **L. Biernacki**, M. Zerihun Demissie, K. B. Workneh, F. Assamnew Andargie, T. Austin. “*Can Trusted Execution Environments be as Powerful as Homomorphic Encryption?*” 48th IEEE/ACM International Symposium on Computer Architecture (ISCA). IEEE/ACM, 2021.
Introduces Sequestered Encryption (SE)—confidential, encrypted computation supported by hardware—and presents a secure coprocessor that abides by five key design axioms to ensure that sensitive data always remains secret
2. **L. Biernacki**, M. Gallagher, Z. Xu, M. Aga, A. Harris, S. Wei, M. Tiwari, B. Kasikci, S. Malik, T. Austin. “*Software-Driven Security Attacks: From Vulnerability Sources to Durable Hardware Defenses*”. ACM Journal on Emerging Technologies in Computing (Special Issue on Emerging Challenges and Solutions in Hardware Security). ACM, 2021.
Proposes a conceptual framework for modeling vulnerability sources as unintended functionality in a program’s transition system, and demonstrates how prominent security attacks/defenses exploit/protect this unintended functionality

Refereed Conference Proceedings

1. **L. Biernacki**, M. Gallagher, V. Bertacco, T. Austin. *“Thwarting Control Plane Attacks with Displaced and Dilated Address Spaces.”* IEEE International Symposium on Hardware Oriented Security and Trust (HOST). Dec 2020.
🏆 **Best Poster Award**
Acceptance rate: $30/104 = 28.8\%$ · *Presents a hardware-based address space randomization defense that protects the code segment by representing code pointers in a superimposed, displaced and dilated address space*
2. M. Gallagher, **L. Biernacki**, S. Chen, Z. Aweke, S. Yitbarek, M. Aga, A. Harris, Z. Xu, B. Kasikci, V. Bertacco, S. Malik, M. Tiwari, T. Austin. *“Morpheus: A Vulnerability-Tolerant Secure Architecture Based on Ensembles of Moving Target Defenses with Churn.”* Proceedings of the Twenty-Third International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS). April 2019.
Acceptance rate: $74/351 = 21.1\%$ · *Presents a secure hardware architecture based on ensembles of moving target defenses with efficient runtime re-randomization*

Non-Refereed Conference Proceedings & Presentations

1. **L. Biernacki**, T. Austin. *“Achieving Data Privacy via Encryption Sequestration in Hardware”* 4th Workshop for Women in Hardware and Systems Security (WISE). Dec 2020. [Abstract, Presentation, Invited Panelist]
Proposes design axioms to ensure the privacy of sensitive data, given trust in hardware, and introduces a Sequestered Encryption (SE) coprocessor that abides by these design axioms
2. **L. Biernacki**, T. Austin. *“Can Trusted Execution Environments be as Powerful as Homomorphic Encryption?”* 5th Workshop on the Future of Computing Architectures (FOCA). Oct 2020. [Presentation]
Discusses design axioms that have the potential to advance microprocessor enclaves forward to the point where they are as powerful as homomorphic encryption, given trusted hardware support
3. **L. Biernacki**, T. Austin. *“Achieving Data Privacy via Encryption Sequestration in Hardware”* Semiconductor Research Corporation (SRC) TECHCON. Sept 2020. [Extended Abstract, Presentation]
Proposes design axioms to ensure the privacy of sensitive data, given trust in hardware, and introduces a Sequestered Encryption (SE) coprocessor that abides by these design axioms
4. **L. Biernacki**, T. Austin. *“Privacy-Enhanced Computer Architectures for Secure Cloud Computing”* The Second Young Architect Workshop (YArch). Mar 2020. [Abstract, Presentation]
Proposes design axioms to realize a confidential computing platform that protects sensitive data on untrusted servers
5. M. Gallagher, **L. Biernacki**, S. Chen, Z. Aweke, S. Yitbarek, M. Aga, A. Harris, Z. Xu, B. Kasikci, V. Bertacco, S. Malik, M. Tiwari, T. Austin. *“Achieving Security with Hardware-Based Puzzles”* 5th Career Workshop for Women and Minorities in Computer Architecture held in association with the International Symposium on Microarchitecture (CWW/MCA—MICRO). Oct 2019. [Poster, Presentation]
Presents a secure hardware architecture based on ensembles of moving target defenses, and frames this approach within a larger conceptual framework of security attacks and defenses

Professional Experience

Center for Applications Driving Architectures (ADA)

Ann Arbor, MI

GRADUATE RESEARCH ASSISTANT, UNIVERSITY OF MICHIGAN

Jan. 2020—PRESENT

- Researching privacy-enhanced computing technologies and their applications, including Trusted Execution Environments (TEEs) and Homomorphic Encryption (HE)
- Developing design axioms that are necessary to ensure the confidentiality of sensitive data in privacy technologies; Designing and optimizing secure architectures that adhere to these design axioms
- Developing privacy-focused benchmarks to measure the performance of competing privacy technologies, including HE

System Security Integrated Through Hardware (SSITH)

Ann Arbor, MI

GRADUATE RESEARCH ASSISTANT, UNIVERSITY OF MICHIGAN

Jan. 2018—Jan. 2020

- Developed a secure RISC-V architecture based on ensembles of moving target defenses with hardware-based runtime re-randomization that obfuscates code, code pointers, and data pointers to defend against control-flow attacks
- Developed a conceptual framework that classifies common security exploits, including control-flow and derandomization attacks, and hardware mitigations

Bentley Systems, Hydraulics and Hydrology Software Product Team

Watertown, CT

SOFTWARE ENGINEERING INTERN

Mar. 2016—Aug. 2016

- Designed and implemented a new component in C# for the hydraulics and hydrology modeling software line that enabled users to create and share design standards for hydraulic models
- Full stack development; Test-driven development practices with agile methodologies and daily Scrum standups

Teaching Experience

Diversity, Equity, and Inclusion in EECS Courses Workshop

WORKSHOP INSTRUCTOR, UNIVERSITY OF MICHIGAN

Ann Arbor, MI

Jan. 2020—Mar. 2020

- Taught new teaching assistants about how to conduct a more inclusive classroom environment, including topics of stereotype threat, implicit bias, and imposter syndrome

EECS 598, Intro to CSE Graduate Studies

PRIMARY INSTRUCTOR, UNIVERSITY OF MICHIGAN

Ann Arbor, MI

Sept. 2019—Dec. 2019

- Founded this course to orient first-year Ph.D. students with graduate studies
- Designed course materials and assignments to introduce students to the skills needed for success
- Presented on various topics including advisor-student relationships, mentoring, and communicating ideas

CSE 2300, Digital Logic Design

PRIMARY LAB INSTRUCTOR, UNIVERSITY OF CONNECTICUT

Storrs, CT

Sept. 2015—May 2017

- Responsible for the instruction of two laboratory sections each semester
- Taught students the software and hardware applications of topics learned in the course, prepared lectures given in lab, and acted as the graduate teaching assistant for this course
- Held weekly office hours, exam review sessions, and graded students' assignments and exams

CSE 1010, Intro to Computing for Engineers

GRADER, UNIVERSITY OF CONNECTICUT

Storrs, CT

Jan. 2015—May 2015

- Responsible for the grading of four laboratory sections, approximately 80 students; Held three hours of office hours weekly, and organized extra problem sessions for students

Service

Research Mentoring & Advising

- 2020 **Mentor**, African Undergraduate Research Adventure (AURA) Ann Arbor, MI
Mentored two undergraduate students from Addis Ababa Institute of Technology, Ethiopia on privacy-preserving architecture research related to Sequestered Encryption
- 2020 **Mentor**, CSEG Graduate Student Mentoring Program Ann Arbor, MI
Mentored a second-year CSE Ph.D. student on success and failure in graduate school
- 2019 **Mentor**, Michigan Engineering Lunch & Lab Graduate Student Mentoring Program Ann Arbor, MI
Mentored two computer science undergraduate students on pursuing graduate school in the discipline
- 2018 **Mentor**, Summer Undergraduate Research Experience (SURE) Ann Arbor, MI
Mentored one undergraduate student from the University of Michigan on computer architecture research related to Morpheus
- 2018 **Mentor**, Michigan Engineering Lunch & Lab Graduate Student Mentoring Program Ann Arbor, MI
Mentored five computer science undergraduate students on pursuing graduate school in the discipline

K-12 Outreach Activities

- 2019 **Primary Instructor**, Discover Engineering Ann Arbor, MI
Created and facilitated a new workshop on Computer Science & Engineering for 8th-10th grade students, exploring how a computer works, basic algorithmic concepts, and touring Michigan research labs
- 2019 **Primary Instructor**, Xplore Engineering Ann Arbor, MI
Facilitated the second iteration of the "A Computer's Heart" workshop for 4th-7th grade students
- 2018 **Instructor**, Girls Who Code (GWC) Ypsilanti, MI
Organized lessons and projects for a local after-school GWC Club, exploring topics like variables and control flow in ProcessingJS, HTML coding, and microcontrollers
- 2018 **Instructor**, Xplore Engineering Ann Arbor, MI
Created and facilitated a new Xplore workshop titled "A Computer's Heart" for 4th-7th grade students, exploring basic computer architecture and machine learning concepts through engaging activities
- 2018 **Volunteer**, Female Excelling More in Math, Engineering, and the Sciences (FEMMES) Capstone Ann Arbor, MI
Volunteered at the FEMMES Capstone event where Michigan graduate students facilitated science-oriented activities for children at the local public library
- 2017 **Lab Instructor**, Seth Bonder Summer Camp in Computational and Data Science Ann Arbor, MI
Designed and facilitated projects in Snap! during this week-long program aimed at teaching computer science to high school students with little or no programming experience

Extracurricular Activities

- 2020 **Co-President**, Ensemble of CSE Ladies (ECSEL+) Ann Arbor, MI
Served as Co-President for this organization whose goal is to support graduate women and gender minorities in CSE; Organized club events and supported fellow officers
- 2020 **DEI Committee Member**, CSE Research Lab Culture & Inclusive Climate Ann Arbor, MI
Served as a student representative on the CSE department's various DEI-focused committees
- 2019 **Officer, Outreach Chair**, CSE Graduate Student Organization (CSEG) Ann Arbor, MI
Organized K-12 outreach opportunities for CSE graduate students; Collaborated with organizations focused on broadening participation in computer science
- 2018 **Officer, Social Chair**, CSE Graduate Student Organization (CSEG) Ann Arbor, MI
Worked to create a sense of community among graduate students via hosting social events for existing and incoming CSE Ph.D. students
- 2017 **Member**, University of Connecticut's Leadership Legacy Storrs, CT
Participated in this highly selective (13 students selected university-wide), year-long leadership program to build on member's legacies as University leaders and prepare them for success beyond graduation
- 2017 **Co-President**, Honors Across State Borders (HASB) Storrs, CT
Organized a week-long alternative spring break trip of more than fifty volunteers; Planned accommodations and service activities, educational pre/post-trip meetings, on-trip discussions, and reflective activities
- 2016 **Officer, Team Leader**, Honors Across State Borders (HASB) Storrs, CT
Lead a team of eight volunteers, within a larger group, during a week-long alternative spring break trip working with Habitat for Humanity; Facilitated discussions on privilege, bias, and other societal issues

Research Program & Organizing Committees

- 2020 **Reviewer**, Design, Automation and Test in Europe Conference (DATE) Grenoble, France
- 2019 **Reviewer**, IEEE/ACM International Symposium on Microarchitecture (MICRO) Columbus, OH
- 2019 **Reviewer**, IEEE International Symposium on Hardware Oriented Security and Trust (HOST) McLean, VA

Skills

- Programming Languages** C/C++, Python, Java
- Architectural Simulation** gem5, QEMU, RISC-V Spike, Pin
- Compiler Extensions** LLVM