Fabrication and Measured Performance of a First-Generation Microthermoelectric Cooler

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***Abstract*—The measured performance of a column-type microthermoelectric cooler, fabricated using vapor-deposited thermoelectric films and patterned using photolithography processes, is reported. The columns, made of p-type Sb_2Te_3 and n-type Bi_2Te_3 with an average thickness of 4.5 μm, are connected using Cr/Au/Ti/Pt layers at the hot junctions, and Cr/Au layers at the cold junctions. The measured Seebeck coefficient and electrical resistivity of the thermoelectric films, which were deposited with a substrate temperature of 130 °C, are -74 $\mu V/K$ and 3.6×10^{-5} $\Omega - m$ (n-type, power factor of 0.15 $mW/K^2 - m$), and 97 $\mu V/K$ and 3.1×10^{-5} $\Omega - m$ (p-type, power factor of 0.30 $mW/K^2 - m$). The cooling performance of devices with 60 thermoelectric pairs and a column width of 40 μm is evaluated under a minimal cooling load (thermobuoyant surface convection and surface radiation). The average cooling achieved is about 1 K. Fabrication challenges include the reduction of the column width, implementation of higher substrate temperatures for optimum thermoelectric properties, and improvements of the top connector patterning and deposition. [1443]**

***Index Terms*—Antimony telluride, bismuth telluride, microthermoelectric cooler, thermoelectric films.**

NOMENCLATURE

A_k	Cross-sectional area of the thermoelectric element (m^2).
d_{te}	Width of the thermoelectric element (m).
J_e	Electrical current (A).
k	Thermal conductivity (W/m-K).
L_{te}	Thickness of the thermoelectric element (m).
N_{te}	Number of thermoelectric pairs.
Q_c	Load heat flow rate (W).
R_e	Electrical resistance (Ω).
$R_{e,c}$	Electrical contact resistance (Ω).
$R_{k,c}$	Thermal contact resistance (K/W).
$R_{k,b,ee}$	Electron boundary resistance (K/W).
$R_{k,b,pp}$	Phonon boundary resistance (K/W).
T	Temperature (K).
Z_e	Figure of merit (1/K).

Greek symbols

α_S	Seebeck coefficient (V/K).
$\Delta\varphi$	Voltage (V).
ρ_e	Electrical resistivity ($\Omega - m$).

Subscripts

c	Cold.
e	Electron.
n	n-type thermoelectric material.
p	p-type thermoelectric material, phonon.
sub	Substrate.
∞	Ambient.

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I. INTRODUCTION

TELLURIDE compounds are the thermoelectric (TE) materials used in the fabrication of the micro-TE cooler, since they currently have the highest cooling performance at room temperature. The techniques used for the synthesis of these compounds are dependent, among other factors, on the desired film thickness. Zou *et al.* [1] deposited thin films (700 nm) of n-type Bi_2Te_3 and p-type Sb_2Te_3 by vapor deposition, which had a room-temperature dimensionless figure of merit Z_eT of approximately 0.3 (optimized, i.e, not including geometric parameters). The Seebeck coefficient α_S and electrical resistivity ρ_e were -200 $\mu V/K$ and 1.29×10^{-5} $\Omega - m$ (power factor of 3.1 $mW/K^2 - m$) for the n-type material deposited at a substrate temperature of 230 °C, and 160 $\mu V/K$ and 3.12×10^{-5} $\Omega - m$ (power factor of 0.82 $mW/K^2 - m$) for the p-type material deposited at 190 °C. Min *et al.* [2] proposed a micro-TE cooler where the TE thin films are grown on a very thin, low thermal conductivity SiC membrane (PECVD) to minimize the heat leakage effect. In their design, the electrical current and heat flow parallel to the film plane. Lim *et al.* [3] deposited thick films (20 μm) of telluride compounds using electroplating for fabrication of TE coolers, where the current and heat flow perpendicular to the film plane (column-type design). They built a microdevice that presented a maximum cooling of 2 K, and Z_eT of 0.011 (which accounts for device geometry). The n-type Bi_2Te_3 films exhibited in-plane Seebeck coefficients ranging from -30 to -60 $\mu V/K$ and an in-plane electrical resistivity of 1×10^{-5} $\Omega - m$. The properties of the p-type $Bi_{2-x}Sb_xTe_3$ films were not fully characterized due to poor reproducibility. Böttner *et al.* [4], depositing 20 μm of telluride compounds by co-sputtering, developed a column-type microcooler using a "two-wafer" concept (n- and p-type materials are first deposited on separated wafers, patterned and then soldered together). This allowed an optimal post-processing of the n- and p-type wafers. A net cooling of 36.7 K has been obtained [5]. The Seebeck coefficient and electrical resistivity are -155 $\mu V/K$ and 2.1×10^{-5} $\Omega - m$ (power factor of 1.14 $mW/K^2 - m$) for the n-type

film, and 227 μV/K and $2.3 \times 10^{-5}\ \Omega - \mathrm{m}$ (power factor of 2.24 $\mathrm{mW/K^2} - \mathrm{m}$, after annealing) for the p-type film.

Several approaches have been proposed to enhance Z_eT in thin film TE materials. Using quantum-confinement effects, which allows the manipulation of α_S by enhancing the density of states near the Fermi energy, Z_eT ranging from 1.3 to 1.6, at 300 K, has been reported for PbSeTe/PbTe quantum dot superlattice structures [6], [7]. Venkatasubramanian *et al.* [8], have shown a Z_eT of 2.4 for p-type nanostructured superlattices of Bi_2Te_3/Sb_2Te_3 at room temperature. These are phonon-blocking/electron-transmitting superlattices, which are produced by alternately depositing thin (1 to 4 nm) films of Bi_2Te_3 and Sb_2Te_3. For n-type $Bi_2Te_3/Bi_2Te_{2.83}Se_{0.17}$, the reported Z_eT is 1.4. Exploring thermionic emission at interfaces, Vashaee and Shakouri [9] have recently shown that metal-base superlattices with tall barriers can achieve a Z_eT larger than 5, at room temperature. A key requirement is the nonconservation of lateral momentum, which allows a higher number of electrons to participate in the thermionic emission process.

Cooling performance of devices based on such nano-engineered TE structures have also been reported. A 1-μm-thick InGaAsP/InGaAsP superlattice-based thin film thermionic emission cooler has demonstrated a maximum cooling of 1.15 K, at room temperature [10]. Fan *et al.* [11], have measured a 2.8 K cooling in a SiGeC/Si superlattice microcooler, at room temperature. Venkatasubramanian *et al.* [8], have shown a net cooling of 32.2 K at room temperature, in a p-type Bi_2Te_3/Sb_2Te_3 superlattice device.

Conventional column-type TE coolers have not been fabricated with thin films (less than 1 μm) due to the parasitic conduction heat transfer between the hot and cold junctions, and the thermal and electrical contact resistances. These problems can be minimized if thicker films (2 to 10 μm) are used. Here, this design is considered for cooling a chemiresistance vapor sensor of a wireless environmental monitor, to increase the sensor sensitivity. As shown in Fig. 1, the thickness of the TE films (Bi_2Te_3 and Sb_2Te_3 used in their simplest form, not doped) is limited to 5 μm (to allow for uniform stoichiometry of the compounds). These films are grown based on the vapor deposition technique of Zou *et al.* [1]. The goal for the cooler is to lower the temperature of the sensor 10 K below ambient in less than 30 seconds, using minimal power with a 3 V battery. The device design is based on predictions from a TE cooler model [12]. The fabrication steps and results from the device characterization of the first generation micro-TE coolers, which include the predicted and measured device performances, are presented and discussed. Fabrication improvements for following device generations are proposed.

II. Device Fabrication

The silicon (Si) wafer used in the fabrication is also the microcooler heat sink. To provide electrical insulation for the device, a 850 nm silicon dioxide layer is grown on the Si wafer. Photoresist (PR) is spun cast, defining a lift-off pattern for the hot (bottom) connectors and electrical connectors (pads). These

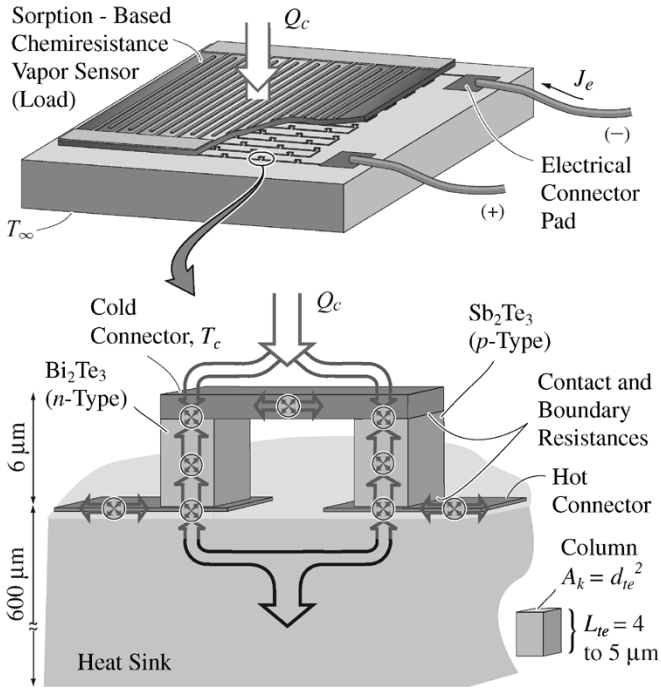

Fig. 1. Rendering of a column-type design micro-TE cooler used with a micro-vapor sensor.

connectors are Cr/Au/Ti/Pt layers grown by e-beam evaporation. The Au and Pt layers are 200 nm and 20 nm thick, respectively. The Cr and Ti are 20 nm thick seed layers. The Pt, which has an electrical resistivity about 5 times larger and a thermal conductivity about 5 times smaller than Au, is used for its good adhesion to the columns, while preventing the diffusion of Au. Each column of the TE element is patterned consecutively before evaporation using an Omnicoat/SU-8 PR mold. SU-8, after exposure and post-exposure bake, becomes a highly crosslinked epoxy, which is extremely difficulty to remove with conventional solvent-based resist strippers. A layer of Omnicoat is deposited prior to SU-8 to facilitate its removal. Omnicoat is developed in an O_2 plasma. Once the TE films have been deposited (in this first generation, with a substrate temperature T_{sub}[1] of 130 °C) as presented in [13], [14], the PR is removed, leaving only the columns on top of the hot connectors, as illustrated in Fig. 2(a). The actual Sb-Te and Bi-Te TE elements deposited on the hot connector pattern are shown in Fig. 2(b) and (c). Note that the width of the TE elements is about 7 μm. The yield of such geometry was below 10% due to the removal of these $7\ \mu\mathrm{m} \times 7\ \mu\mathrm{m}$ TE elements with the photoresist during the lift-off process. Only devices with TE element cross-sectional area of $40\ \mu\mathrm{m} \times 40\ \mu\mathrm{m}$ (which presented 90% yield at this point in fabrication) were completed.

The final steps of the fabrication process are summarized in Fig. 3. A contact area is defined on top of each TE element [see Fig. 3(a)]. After developing and hardbaking the PR (AZ9245), a thin Cr/Au layer (20 nm/20 nm) is deposited by sputtering. This metallization is necessary to avoid the exposure of the PR in the

[1]Depositions with a T_{sub} greater than or equal to 170 °C resulted in an over hardbaked PR, which could not be removed without damaging the thermoelectric films. In the first generation, a safe value of 130°C was used for T_{sub} to allow for a higher device yield.

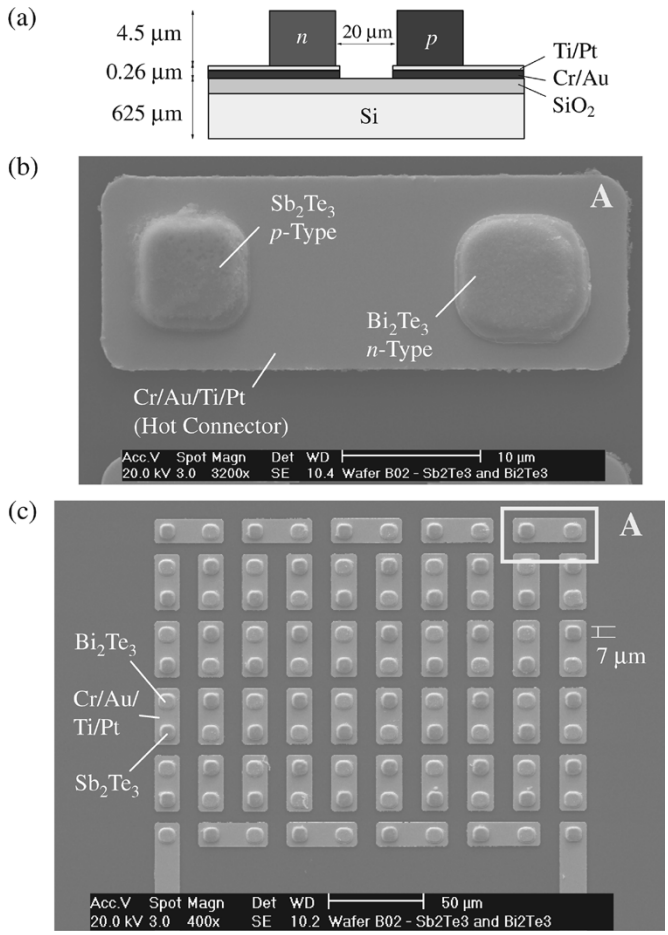

Fig. 2. Bi_2Te_3 and Sb_2Te_3 films deposited on Cr/Au/Ti/Pt hot (bottom) connectors. The cold (top) connectors are not shown. (a) Sketch showing the approximate thickness of the films. (b) SEM micrograph showing a top view of the fabricated structures. This image is the enlarged section "a" indicated in the part (c), top right. (c) SEM micrograph of a device with 50 TE pairs.

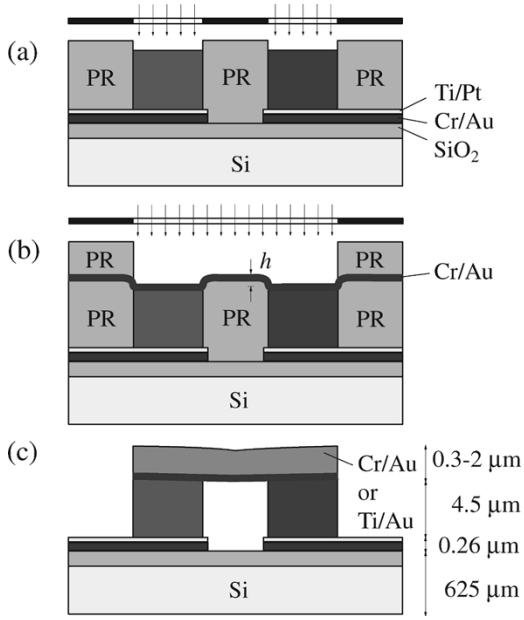

Fig. 3. Schematic outlining the procedure for fabrication of the cold (top) connectors. (a) Contact opening for Cr/Au. (b) Contact opening for Au. (c) Structure that will be connected to a microsystem (load).

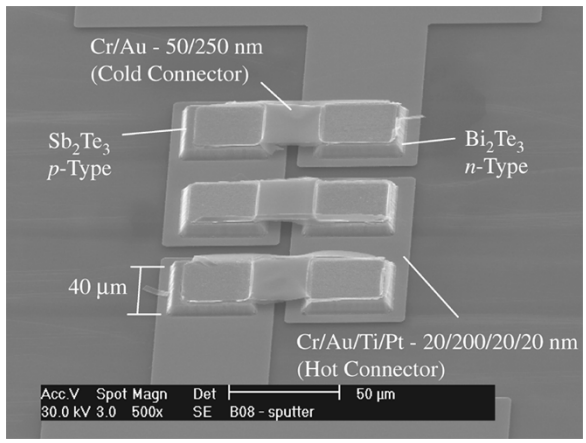

Fig. 4. SEM micrograph showing a complete electrically connected device with 3 TE pairs, where the top connector was deposited by sputtering (Cr/Au, 50/250 nm). The cross-sectional area of the TE columns is equal to $40\ \mu\mathrm{m} \times 40\ \mu\mathrm{m}$. The thicknesses of the n- and p-type elements are given in Table I.

subsequent photolithography process [see Fig. 3(b)], which is required to define the area where Au (the metal that forms the cold connectors and closes the electrical circuit of the TE cooler) is deposited [see Fig. 3(c)]. This structure will be connected to a load. To ensure a clean electrical contact opening, the PR on top of the columns is overexposed. This is due to variations in the PR thickness, caused by differences in the height of the TE elements (differences as large as 0.8 μm between the n- and p-type TE elements have been observed). Using Ti/Cu and Cu for the last two metallizations (hot connector) results in a large increase in the total electrical resistance of the devices with time, which might be due to oxidation of the Cu.

The height of the PR above the columns, indicated by h in Fig. 3(b), ranges from 1 to 2 μm. Due to this surface nonuniformity, two techniques have been tested for the deposition of the top connector. First, using sputtering (which allows a good step coverage), the top connector was formed by a thin layer of Cr/Au (50 nm/250 nm). In other trials, using evaporation, a thicker layer, Ti/Au (1500 nm/500 nm), was needed. In Figs. 4 and 5, the results of the cold connector fabrication by sputtering and by evaporation are shown, respectively, where the PR layers [indicated in Fig. 3(b)] were successfully removed with lift-off in acetone. Note that in Fig. 4 there are undesired residual materials left on the top connectors (which cause poor thermal contact with the load). This is due to the Cr/Au that is grown on the side walls of the PR mode. Here there is a compromise between decreasing the PR thickness, and allowing enough PR height for the lift-off.

III. Device Characterization

The cooling performance of the fabricated micro-TE coolers has been evaluated at an ambient temperature T_∞ of 63 °C (all devices discussed here were fabricated on the same wafer). The TE properties, composition and crystal structure of the n- and p-type films that compose these devices were investigated. From

TABLE I
DEPOSITION CONDITIONS AND MEASURED PROPERTIES OF Bi_2Te_3 AND Sb_2Te_3 FILMS (AT ROOM TEMPERATURE)

TE Film	Sb_2Te_3	Bi_2Te_3
T_{sub}, °C	130	130
L_{te}, μm	4.2	4.9
ρ_e, $\mu\Omega$-m	31	36
α_S, μV/K	97	-74
at%Te/at%(Bi or Sb)	1.0	1.9

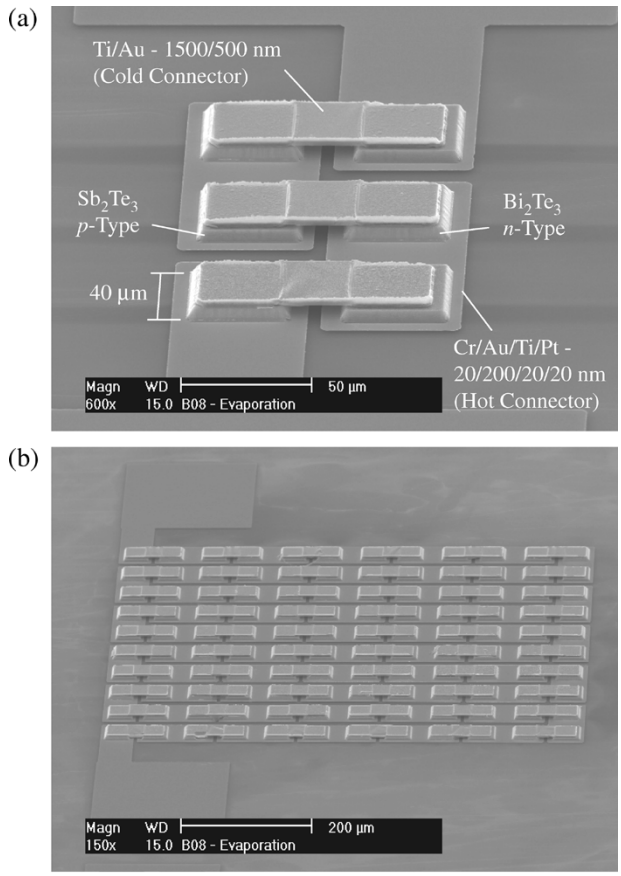

Fig. 5. SEM micrograph showing complete electrically connected devices with (a) 3 and (b) 60 te pairs. The top connectors were deposited by evaporation (Ti/Au, 1500/500 nm). The cross-sectional area of the columns is equal to $40\ \mu\mathrm{m} \times 40\ \mu\mathrm{m}$. The thicknesses of the n- and p-type elements are given in Table I.

a TE cooler model [12], the cooling performance was predicted and compared with the measured results.

A. *Properties of* Bi_2Te_3 *and* Sb_2Te_3 *Films*

The measured substrate temperature during the film deposition (T_{sub}), thickness (L_{te}), electrical resistivity (ρ_e), Seebeck coefficient (α_{S}) and stoichiometry (at% element ratio) of the n- and p-type TE elements are given in Table I. The measurement techniques have been discussed in [13], [14]. In Fig. 6, reference diffraction patterns from powdered single crystals of Bi_2Te_3

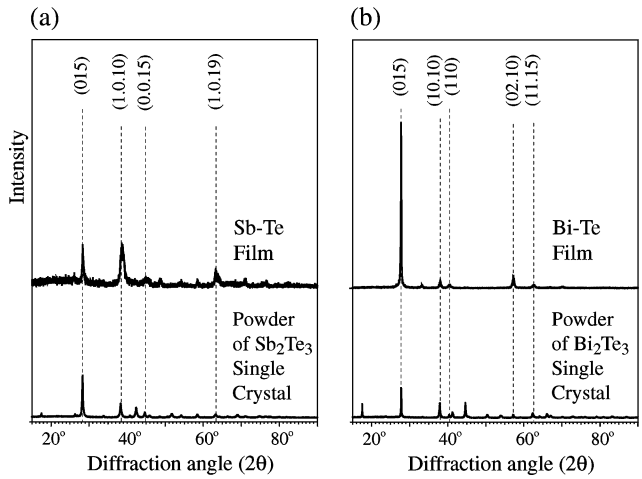

Fig. 6. X-ray diffraction pattern of co-evaporated films and powdered single crystals of (a) Sb_2Te_3 and (b) Bi_2Te_3. The measured peaks agree with the powder diffraction file [16].

TABLE II
BASE-LINE PROPERTIES USED IN THE TE COOLER MODEL [12]

TE Film	Sb_2Te_3	Bi_2Te_3
k, W/m-K	2.1	2.0
$(A_kR_k)_c$, K/(W/m^2)	10^{-7}	10^{-7}
$(A_kR_e)_c$, Ω-m^2	2×10^{-11}	2×10^{-11}
$(A_kR_k)_{b,pp}$, K/(W/m^2)	8.0×10^{-8}	9.2×10^{-8}
$(A_kR_k)_{b,ee}$, K/(W/m^2)	9.3×10^{-7}	3.5×10^{-7}

and Sb_2Te_3 are compared with the diffraction patterns of the co-evaporated films. The data agree with the associated entries in the Powder Diffraction File [16], and the corresponding reflection planes (hkl) are labeled. Although the films are off-stoichiometry (at% element ratio $\neq 1.5$), the position of the peaks in the films match with the reference patterns. The results show that the films are polycrystalline without a strong preferential orientation. This justifies using the measured in-plane TE properties as the cross-plane properties in the modeling for prediction of the device cooling performance.

The figure of merit Z_e is given by [15]

$$Z_e = \frac{(\alpha_{S,p} - \alpha_{S,n})^2}{\left[(k\rho_e)_p^{\frac{1}{2}} + (k\rho_e)_n^{\frac{1}{2}}\right]^2} \tag{1}$$

where k is the thermal conductivity of the TE element listed in Table II. Note that this is a optimized expression for Z_e since it does not include geometric parameters. At room temperature, the dimensionless figure of merit Z_eT was found to be 0.032.

B. *Predicted Cooling Performance*

In [12], the transport of heat and electricity in a micro-TE cooler have been analyzed. Consideration was given to the phonon $(A_kR_k)_{b,pp}$ and electron $(A_kR_k)_{b,ee}$ boundary resistances, the phonon-electron thermal nonequilibrium in the regions adjacent to the interfaces of the TE elements, and

the thermal $(A_k R_k)_c$ and electrical $(A_k R_e)_c$ contact resistances. Using the measured ($L_{\rm te}$, ρ_e and $\alpha_{\rm S}$) and base-line properties given in Tables I and II, respectively, the performance of a device with the number of TE pairs $N_{\rm te}$ equal to 60 and a cross-sectional area of the columns A_k $(= d_{\rm te}^2)$ of $40\ \mu{\rm m} \times 40\ \mu{\rm m}$, was evaluated. The predicted device total electrical resistance R_e is 50 Ω, and the maximum temperature difference between the heat sink and the top connector[2] $(T_\infty - T_c)$ is 0.5 K, for an applied voltage (potential) $\Delta\varphi$ of 1.8 V, an electrical current J_e of 36 mA, and under a minimal cooling load Q_c of 0.1 mW (thermobuoyant surface convection and surface radiation).

C. Measured Cooling Performance

Using an infrared thermal microscope (InfraScope II) and 5x lens (pixel resolution of 4.8 μm and accuracy of 5%), the thermal image of a fabricated micro-TE cooler ($N_{\rm te}$ of 60 and $d_{\rm te}$ of 40 μm) operating at a J_e of approximately 23 mA was obtained, and is shown in Fig. 7. The measured R_e of this device (at room temperature) was 51 Ω. Temperature calibration was performed by measuring the surface emissivity at different temperatures, and fitting a linear function to the measured points [17].

Note that, in the graph of Fig. 7, a side-view schematic drawing of the TE pairs (scaled with respect to pixels) indicates the position of the line trace in the thermal image. Darker lines, which indicate lower temperatures, are above the TE elements, while the surfaces of the bottom connectors and the substrate $({\rm SiO_2})$ are marked by higher temperatures. In this case, $(T_\infty - T_c)$ can be approximated to 1.3 ± 0.5 K, where T_∞ is maintained at about 63 °C. The thermoelecric cooling figure of merit can be obtained from [15]

$$Z_e = 2\frac{(T_\infty - T_c)}{T_c^2}. \tag{2}$$

For T_c equal to 61.7 °C, $Z_e T_\infty$ is found to be 0.0078 (four times smaller than the optimized $Z_e T$ calculated in Section III-A).

In the thermal image, the isolated spots with large temperature gradients indicate fabrication defects. This device had the top connectors deposited by sputtering, and, as shown in Fig. 4, there are residual metals not completely removed by the lift-off process. These can cause an electrical short-circuit between the top and bottom connectors. The nonuniform temperatures observed at the top connectors can be due to the TE element surface roughness or oxidation, both of which compromise an efficient thermal contact.

A second device, also with $N_{\rm te}$ of 60, $d_{\rm te}$ of 40 μm, and with the top connector deposited by sputtering, was annealed at 200 °C for 2 hours in a nitrogen stream. The measured R_e before and after annealing were 51 Ω and 58 Ω, respectively. A thermal image of this device is shown in Fig. 8. Observe the difference in the lay-out of the TE elements and connectors along lines 1 and 2 (shown by the side-view schematic drawings superimposed on the temperature graphs). The line trace 2 marks the complete

[2]The temperature difference $(T_\infty - T_c)$ is also referred in the text as the device cooling performance. The coefficient of performance, which is the ratio between the cooling load Q_c and the electrical power, is nearly zero, since Q_c is minimal.

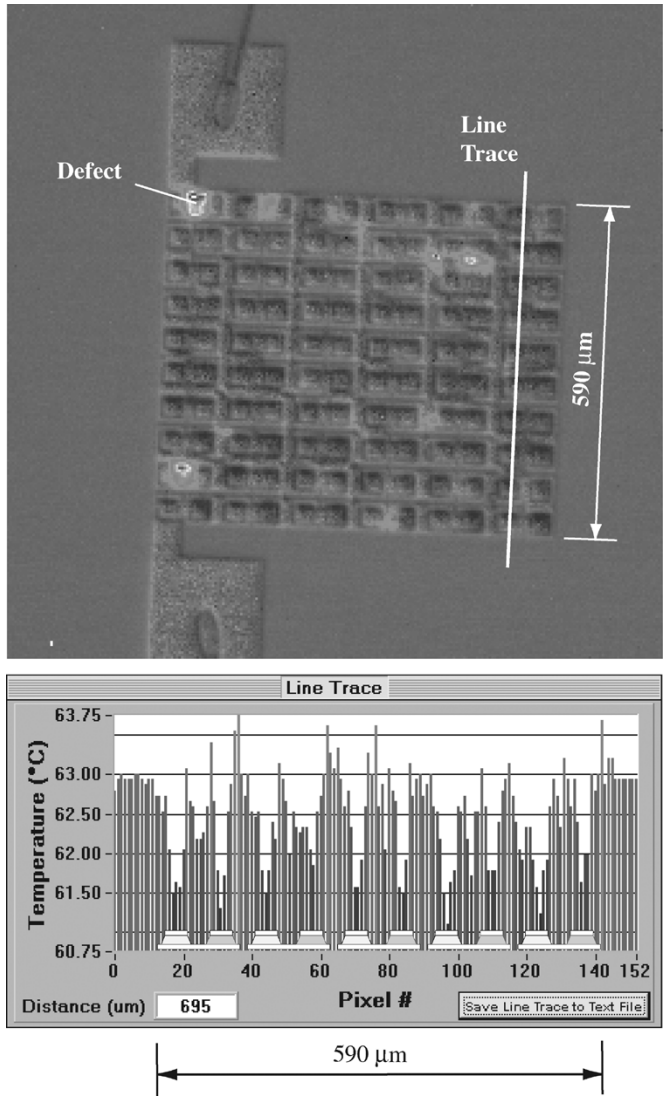

Fig. 7. Infrared surface thermal image of a device with 60 TE pairs and column width of 40 μm. The top connectors were deposited by sputtering. The layout of the TE elements and connectors along line-trace is represented by the sideview schematic drawing at the temperature graph.

extension of the top connectors, where lower temperatures, although not uniform, are evident. In this case, $(T_\infty - T_c)$ can be approximated as 0.8 ± 0.5 K (where T_∞ is maintained at about 62.5 °C), indicating that annealing (at the conditions mentioned above) did not significantly affect the overall device cooling performance when compared with the first device tested. However, note that this was a preliminary attempt on improving the performance by thermal post-treatment. A more careful investigation on annealing is required for each of the TE films (n- and p-type) aiming at improvement of the TE properties. Also, annealing the device, can reduce the contact resistances. In this regard, the inclusion of a diffusion barrier between the TE elements and metal connectors should be considered.

The micro-TE coolers with the top connectors deposited by evaporation presented an overall electrical resistance 1.6 to 1.8 times the R_e of the devices previously discussed (i.e., devices with top connectors deposited by sputtering), and it increased up to 5 times after annealing at 200 °C for 2 h in a nitrogen stream.

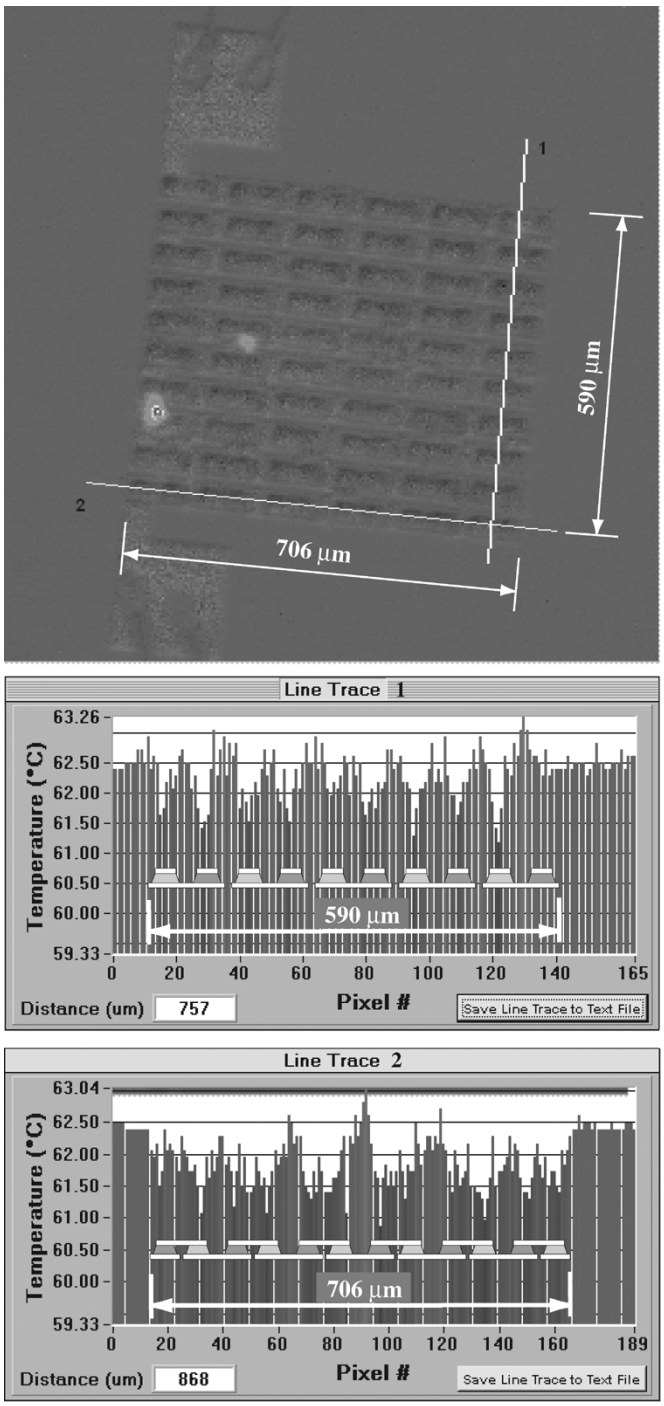

Fig. 8. Infrared surface thermal image of a device with 60 TE pairs and column width of 40 μm, which was annealed at 200 °C for 2 h. The top connectors were deposited by sputtering. The layouts of the TE elements and connectors along lines 1 and 2 are represented by the side-view schematic drawings at the temperature graphs.

These devices produced no detectable cooling. This might be due to the diffusion of the thick Ti layer (1.5 μm, deposited prior to Au) into the TE elements.

D. Comparison Between Measured and Predicted Cooling Performances

The characterized devices have an overall electrical resistance about 2% (before annealing) to 16% (after annealing) larger than

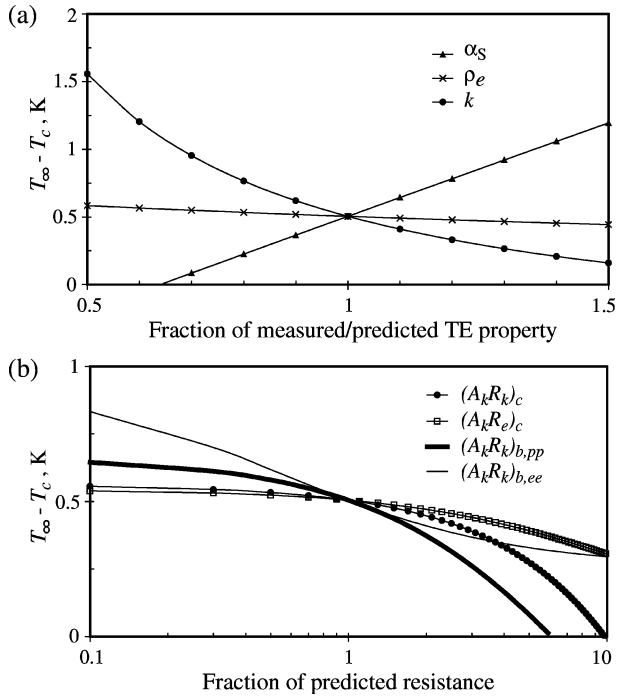

Fig. 9. Effect of (a) TE properties and (b) resistances used in the TE cooler model on the predicted cooling performance of a device with 60 TE pairs and column width of 40 μm.

the predicted resistances. The measured device temperature difference $(T_\infty - T_c)$ was approximately 100% larger than the predicted value. The defects observed as hot spots in the thermal images indicate that improvements can be made in the fabrication of the top connectors, which would increase the disagreement between the measured and predicted performances.

The properties used in the TE cooler model [12], which are given in Tables I and II, present uncertainties that can be related to this difference. It is possible that the TE properties of the films have changed during the top connector fabrication process, where the wafer was heated to as high as 200 °C. The sensitivity of the device overall performance to the TE properties and thermal and electrical resistances is shown in Fig. 9(a) and (b), for $\Delta\varphi$, Q_c, T_∞, $N_{\rm te}$ and $d_{\rm te}$ equal to 1.8 V, 0.1 mW, 63 °C, 60 pairs and 40 μm, respectively. The TE properties are varied up to $\pm$50% of their base values and the resistances are varied from a factor of 0.1 to a factor of 10.

Note that, from Fig. 9(a), the relation $\alpha_S^2/(\rho_e k)$ (a measurement of the TE element performance) is not obeyed. This is due to the TE element geometry being far from optimum ($L_{\rm te}/d_{\rm te}$ around unity). The TE properties most affecting performance are α_S and k. In Fig. 9(b), it is seen that the device performance is less sensitive to the electrical than to the thermal resistances (boundary and contact).

IV. Proposed Fabrication of Future Generations

Developments in the fabrication of a micro-TE cooler comprise overcoming the limits encountered with the processes indicated in Fig. 10. The first-generation device fabricated and tested, whose results were presented in previous sections, is labeled as GEN-1. In this first generation, a limit on the TE column length $L_{\rm te}$ (indicated in the inclined axis of Fig. 10)

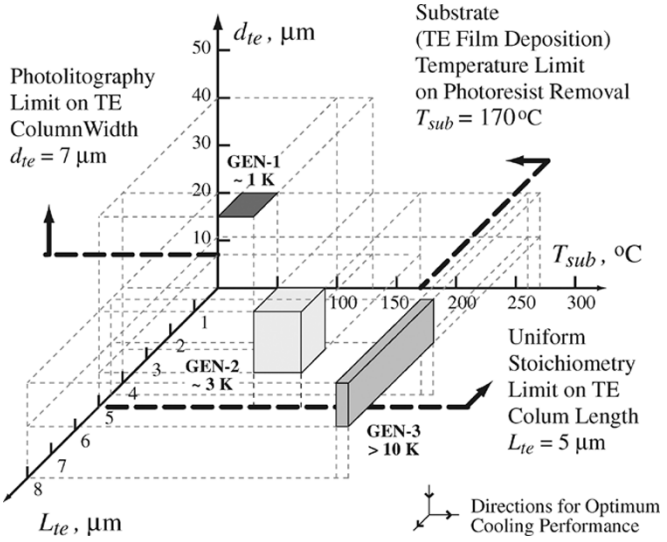

Fig. 10. Map of device generation aiming at GEN-3. GEN-1 has been completed. GEN-2 is the next generation of devices.

was reached due to difficulty in controlling the sublimation of the tellurium element. The uncertainty in the deposition rate increases with the depletion of Te inside the evaporation boat. When this fluctuation is greater than $\pm 0.6\,\text{Å/s}$ (for films thicker than 5 μm), large stoichiometry nonuniformity is generated. Also in GEN-1, the column width of the TE elements (indicated in the vertical axis) was restricted to 40 μm. Almost no yield of smaller d_{te} devices was obtained, as discussed in Section II. The TE films were deposited at low T_{sub} (indicated in the horizontal axis) to facilitate the PR removal.

GEN-2 focuses on increasing the ratio $L_{\text{te}}/d_{\text{te}}$ (0.11 for GEN-1) toward unity. As the TE element length has reached a limit of 5 μm (uniform stoichiometry limit), improvements can be made in the photolitography process to allow for a smaller d_{te}. The performance of the TE films can be improved (α_S^2/ρ_e can be doubled) by a slight increase in T_{sub}, from 130 °C in GEN-1 to maximum of 170 °C in GEN-2 (limited by the PR removal), as indicated in the horizontal axis of Fig. 10, and also by stoichiometry optimization. In the cold connector fabrication, the thickness of the second metallization should be increased (minimum of 2 μm) to allow for lower R_e. The maximum predicted cooling performance for GEN-2 is 3.1 K, for $\Delta\varphi$ of 2.2 V.

GEN-3 will focus on the fabrication of high performance TE elements, either by patterning the high performance TE films (deposited at optimal conditions, i.e, $230\,^\circ\text{C} < T_{\text{sub}} < 260\,^\circ\text{C}$, as indicated in the horizontal axis of Fig. 10) [13], [14], or by post-processing (e.g., annealing) the films deposited at low substrate temperature to improve their TE performance. For L_{te} of 4.5 μm, $(T_\infty - T_l)$ as high as 10.4 K is predicted for $\Delta\varphi$ of 6 V. Increasing L_{te} to 8 μm, this performance can be increased by 42%, to $(T_\infty - T_l)$ of 14.8 K.

V. Summary

Micro-TE cooler devices with 60 TE pairs, and thickness and width of columns of approximately 4.5 μm and 40 μm, respectively, were fabricated using co-evaporation for deposition of the TE elements. The Seebeck coefficient and electrical resistivity of the films were measured, and from a micro-TE cooler model a net cooling of 0.5 K was predicted for an applied voltage of 1.8 V and minimal cooling load of 0.1 mW. The predicted total electrical resistance R_e was 50 Ω.

Using an infrared camera, thermal images of these devices operating at 23 mA and at an ambient temperature of 63 °C were obtained. An average cooling performance of 1.3 ± 0.5 K was verified (measured R_e of 51 Ω). For a device with same geometry and TE properties, which was annealed at 200 °C for 2 hours, the cooling performance was 0.8 ± 0.5 K. After annealing, the electrical resistance increased to 58 Ω, which is an indication of need for a diffusion barrier between the metal connectors and TE elements.

For increasing performance, future generations of devices should focus on the deposition and patterning of high performance TE films, fabrication of TE elements with optimal aspect ratio $L_{\text{te}}/d_{\text{te}}$, and realization of minimal contact resistances at the device interfaces.

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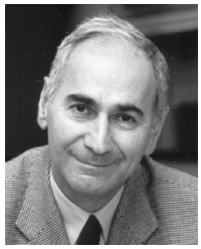

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