Multistage Planar Thermoelectric Microcoolers

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***Abstract*—Many types of microsystems and microelectromechanical systems (MEMS) devices exhibit improved performance characteristics when operated below room temperature. However, designers rarely pair such devices with integrated cooling solutions because they add complexity to the system and often have power consumption which far exceeds that of the microsystem itself. We report the design, fabrication, and testing of both one- and six-stage thermoelectric (TE) microcoolers that target MEMS applications through optimization for low-power operation. Both coolers use thin-film Bi_2Te_3 and Sb_2Te_3 as the n- and p-type TE materials, respectively, and operate in a planar configuration. The six-stage cooler has demonstrated a $\Delta T = 22.3\,^{\circ}\mathrm{C}$ at a power consumption of 24.8 mW, while the one-stage cooler has demonstrated a $\Delta T = 17.9\,^{\circ}\mathrm{C}$ at a lower power consumption of 12.4 mW. [2011-0087]**

***Index Terms*—Microcooler, microelectromechanical systems (MEMS), solid-state cooling, thermoelectric (TE) devices.**

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I. Introduction

THE NEED for microscale coolers is driven by microelectromechanical systems (MEMS) and electronic devices, such as resonators, gyroscopes, infrared sensors, and low-noise amplifiers, which exhibit enhanced performance when operated at temperatures below ambient. Resonant MEMS, in particular, have very low power dissipation, and many of the applications that integrate them seek to exploit these low-power features as well as their small size [1]. As a result, any cooling device designed for integration with these low-power MEMS devices should itself be both low power and compact.

One approach to microscale cooling has been the development of miniaturized Joule–Thompson (J–T) coolers [2]–[6]. Some of these devices have effectively produced temperature differentials of 192 K with heat loads up to 16 mW, using a heat exchanger with a size of $2\ \mathrm{mm} \times 35\ \mathrm{mm} \times 1\ \mathrm{mm}$ [2]. However, the heat exchanger alone does not define a complete J–T cooling system. J–T coolers also require a source of compressed gas, which can be supplied by an external pressurized source [3] or by an attached compressor [7]. The lack of small simple implementation makes J–T coolers impractical for many microcooling applications.

Thermoelectric (TE) cooling, although less efficient than J–T cooling, relies on solid-state operating principles that can be scaled to the microdomain. As a result, TE cooling can be effectively utilized in applications that require small, simple, and robust coolers. Additionally, TE materials can be deposited and patterned at the wafer level with standard microfabrication techniques, making batch-mode production a possibility. Microscale TE coolers have been previously demonstrated by several groups [8]–[18] representing a wide range of choices in cooler design, TE materials, and fabrication techniques. A summary of devices from industry and academia is provided in Table I. The best performing coolers in this group are able to generate temperature differentials between 40 K and 100 K; however, they require power inputs of several hundred milliwatts or more. Such high power consumption makes these coolers incompatible with MEMS integration in many applications. On the other hand, the low-power coolers to date have not demonstrated enough total temperature differential to be useful in achieving meaningful performance gains from the target electronics and MEMS devices. This paper presents a TE microcooling solution that can generate reasonably large temperature differences with very small power.

The special features of micro TE coolers, including size effects and interfacial transport phenomena, are addressed in [19].

TABLE I
PREVIOUS WORK IN TE MICROCOOLERS

Reference	[8]	[13]	[18]	[14]
Structure	1-Stage Vertical	1-Stage Vertical	1-Stage Planar	3-Stage Vertical
Materials	*n*-Bi_2Te_3/$Bi_2Te_{2.83}Se_{0.17}$ *p*-Bi_2Te_3/Sb_2Te_3	*n*-Bi_2(Se,Te_3) *p*-(Bi,Sb)$_2Te_3$	*n*-Bi_2Te_3 *p*-Sb_2Te_3	*n*-Bi_2Te_3/$Bi_2Te_{2.83}Se_{0.17}$ *p*-Bi_2Te_3/Sb_2Te_3
ZT	*n*-type: 1.4 *p*-type: 2.4	*n*-type: 0.53 *p*-type: 0.71	*n*-type: 0.5 *p*-type: 0.84	*n*-type: 1.4 *p*-type: 2.4
Cooling at optimum input current; ambient temperature	55 K @ 3.9 A	48 K @ 2.2 A; 85°C	5 K @ 4 mA	102 K. Current varies by stage.
Estimated power consumption	362 mW	Unknown	0.33 mW	5 W (minimum)
Estimated extrinsic *ZT*	0.54	0.31	0.034	NA

The maximum temperature difference that a thermocouple (TC) can achieve in the absence of parasitic effects is given by [20]

$$\Delta T_{\max} \equiv (T_h - T_c)_{\max} = \frac{ZT^2}{2} \tag{1}$$

where T_c is the cold junction temperature and Z is the TE figure of merit for a pair of materials, i.e.,

$$Z = \frac{(\alpha_{S,p} - \alpha_{S,n})^2}{\left[(\kappa_p \rho_{e,p})^{1/2} + (\kappa_n \rho_{e,n})^{1/2}\right]^2} \tag{2}$$

where κ_t is the thermal conductivity, $\alpha_{S,i}$ is the Seebeck coefficient, and $\rho_{e,i}$ is the electrical resistivity (i indicates the p- or n-type material). For the case where the n- and p-type materials have identical material properties with the exception of the sign of the Seebeck coefficient, the figure of merit reduces to

$$Z = \frac{\alpha_S^2}{\rho_e \kappa}. \tag{3}$$

By itself, (1) does not indicate any influence of scaling on the performance of the cooler. All properly proportioned coolers can theoretically reach the maximum ΔT described in (1). However, the current needed to achieve $\Delta T_{\max}$ for a given set of materials does scale with the dimension of the cooler. The current needed to reach $\Delta T_{\max}$ is

$$I_{\text{opt}} = \frac{\alpha_S T_c}{R_e} \tag{4}$$

where α_S is the Seebeck coefficient and R_e is the total electrical resistance of one TE pair (or TC). In a vertical cooler, R_e is proportional to δ_{TE}, the thickness of the TE films. As a result, the power consumption at I_{opt} and $\Delta T_{\max}$ becomes

$$P_e = 2I_{\text{opt}}^2 R_e + 2\alpha_S I_{\text{opt}} \Delta T = \frac{2\alpha_S^2 T_c T_h}{\rho_e} \left(\frac{\delta_{\text{TE}}}{A_{\text{TE}}}\right)^{-1} \tag{5}$$

where A_{TE} is the cross-sectional area of the TC. From (5), we note that the power consumption at $\Delta T_{\max}$ scales inversely with the aspect ratio of the TE elements $\delta_{\text{TE}}/A_{\text{TE}}$. Therefore, coolers with a high temperature differential and low power consumption require TE elements with a high aspect ratio. Achieving high aspect ratios with thin films requires a planar design that transports heat laterally in the plane of the film, instead of vertically through the film. This orientation of the TCs allows for lithographic definition of the TE aspect ratio and makes TE elements of arbitrary design possible. This stands in contrast to the vertical design where the maximum aspect ratio is limited by the maximum film thickness and the minimum lateral feature size. While using a lateral design makes low-power design with thin-film TE materials a possibility, the achievable temperature differential is still limited by the figures of merit of the materials being used. To overcome this limitation, multiple stages can be employed [21]. A multistage cooler should meet three basic criteria in order to be effective. First, as with a single-stage cooler, there must be low thermal conductance across each stage. Second, the first stage (the warmest) must have a higher heat removal capacity than the second stage, the second stage must have a higher heat removal capacity than the third, and so on. This is necessary because the Joule heating that occurs in a given stage acts as a thermal load on all the stages below it. For example, in a two-stage cooler, the second stage experiences only the thermal load dissipated by the device being cooled. Stage one, on the other hand, experiences a thermal load equivalent to the power dissipated in the target device plus the power dissipated in the second stage of the cooler. It must therefore be able to remove more heat than the second stage. Finally, there must be a high thermal conductance between consecutive stages. This is necessary to evenly distribute the heat transported into the interstage region by the higher stage to all the TCs of the lower stage. At the macroscale, a typical structure used to realize multistage coolers is a vertical pyramid, with the coldest stage at the peak [22]. The shape arises naturally from the need for more cooling power at the lower stages. The bulk TE material forms the structure of the pyramid, eliminating the need for any additional materials to span stages and minimizing parasitic thermal conduction. A high-thermal-conductivity ceramic is used as the thermally conductive interstage material. This technique has seen limited but effective implementation at the microscale with devices demonstrating $\Delta T_{\max} = 102$ K [14]. However, we estimate that these vertical structure devices consume a minimum of 5.3 W. This estimate is based on resistive losses in the TE materials using the resistivity figures published in [23] and the dimensions and currents given in [14]. As with a single-stage cooler, adapting the multistage design to a planar structure will allow for a decrease in power consumption of up to two orders of magnitude. Therefore, we have implemented a multistage architecture using a planar design by arranging

TABLE II
TE PROPERTIES AND DEPOSITION CONDITIONS

Material	Sb_2Te_3	Bi_2Te_3
Substrate	Silicon Oxide	Silicon Oxide
Substrate Temperature	232°C	260°C
Deposition Rate (Å/s)	Sb: 1	Bi: 1
	Te: 3	Te: 2.4
Electrical Resistivity (μΩ·m)	12.9	20.2
Seebeck Coefficient (μV/K)	160	-210
Calculated ZT at 300K *	0.39	0.43

* assuming κ =1.5 W/m·K based on fitting described in Section V.

the stages in a series of concentric rings (or polygons), with the coldest stage at the center. The remainder of this paper will discuss the materials and microstructures used to realize a planar multistage TE microcooler, investigate the impact of parasitic effects on the performance of multistage planar coolers, and present test results from several different cooler designs.

II. MATERIALS AND DEPOSITION

At the macroscale, the TE materials of choice for cooling in the range of 300 K are ternary and quaternary alloys of $(Bi, Sb)_2(Te, Se)_3$, sometimes with additional dopants. In bulk form, these materials have been produced with demonstrated ZT at 298 K as high as 1.26 for p-type $(Bi_{0.25}Sb_{0.75})_2Te_3$ doped with excess tellurium and 1.19 for n-type $Bi_2(Te_{0.94}Se_{0.06})_3$ doped with iodine and excess tellurium [24]. Thin films of $(Bi, Sb)_2(Te, Se)_3$ with uniform composition can be deposited by a variety of methods, including electroplating [26], sputtering [27], and coevaporation [28], [29]. These techniques have produced TE materials with ZT values that approach those found in bulk materials of similar composition. Recently, superlattice materials consisting of alternating layers of various $(Bi, Sb)_2(Te, Se)_3$ compounds have been deposited by metal–organic chemical vapor deposition, yielding ZT values as high as 2.4 for n-type material and 1.4 for p-type material [25]. For this project, coevaporated binary compounds were utilized. The materials were deposited on heated substrates from independently controlled elemental sources to achieve near-stoichiometric films. The films have been previously characterized, and the parameters of deposition have been optimized for maximum ZT [29]. The deposition conditions and resulting film properties are summarized in Table II. The n-type Bi_2Te_3 has a ZT of 0.43, while the p-type Sb_2Te_3 has a ZT of 0.39, both of which are comparable to properties achieved by others in binary thin films.

III. STRUCTURE AND FABRICATION

To create a planar multistage TE microcooler, a microfabricated structure was developed which meets the criteria for effective multistage cooling. The cooler is shown in Fig. 1. It utilizes a multiwafer stack of silicon and glass. The two substrates are processed in parallel and are then bonded together to form the completed cooler.

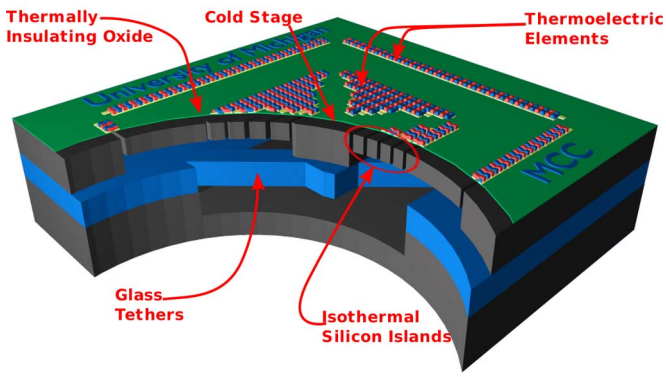

Fig. 1. Three-dimensional rendering of the six-stage TE microcooler showing its major components, including the isothermal silicon islands, insulating dielectric, supporting glass, and TE elements.

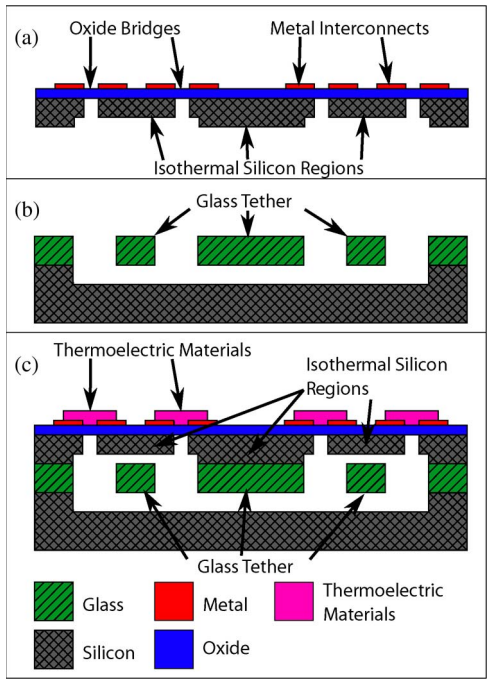

Fig. 2. (a) Cross-sectional view of the "thermal substrate" fabricated from a 100-μm-thick silicon wafer. (b) Cross-sectional view of (middle) "structural substrate," which contains a suspended glass tether used to support the cold stage. (c) Cross-sectional view of the completed cooler.

A. Thermal Substrate

The top substrate in the stack is fabricated from a thin silicon wafer and implements the necessary thermal properties for a multistage cooler. The interstage regions are made of silicon, which has high enough thermal conductivity to make these regions isothermal. In the vertical pyramid design, only the TE materials span the space between the isothermal interstage layers. Thin-film planar TE coolers require an additional material to span this gap and mechanically support the TE films. Here, we use a thin dielectric membrane to serve this function without creating a large parasitic heat path between stages. The top substrate is fabricated using the following steps, as shown in Fig. 2(a).

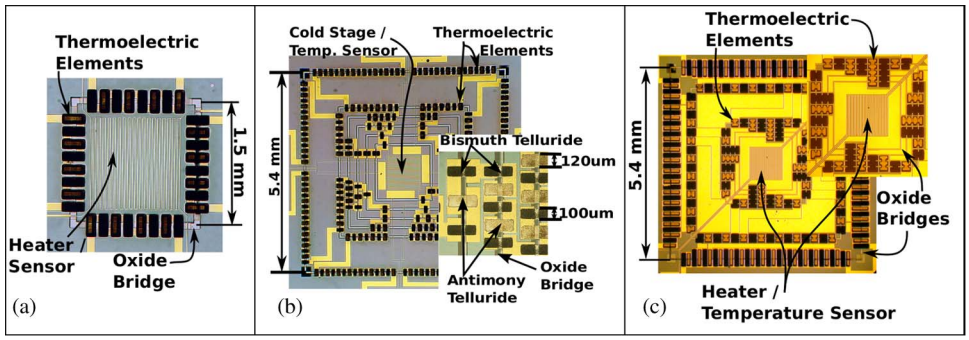

Fig. 3. Top-down micrographs of (a) a one-stage cooler, (b) the Version-1 six-stage cooler with visible cold stage, isothermal islands, and TE elements, and (c) the Version-2 six-stage cooler, with a different isothermal island spacing and a different TE element configuration from (b). The insets highlight the TE elements and oxide bridges.

1) A thin film of silicon dioxide is deposited on the top surface of the wafer and patterned by etching in buffered hydroflouric acid.
2) A layer of Cr/Au is deposited on top of the oxide layer and patterned using lift-off.
3) A 30-μm recess is etched in the back side of the wafer using deep reactive ion etching (DRIE).
4) A second DRIE step creates deep through-wafer trenches that stop on the SiO_2 layer. The trench etching forms concentric squares of silicon separated by oxide bridges, as shown in Fig. 3.
5) Both the front and back sides of the wafer are cleaned using O_2 plasma.

B. Structural Substrate, Bonding, and TE Deposition

Because the resulting thermal substrate is relatively fragile, a second substrate, referred to here as the structural substrate, is fabricated to provide additional mechanical support without sacrificing overall thermal isolation. The support is provided by a thin glass tether, which is bonded to the center of the cooler and/or selected isothermal rings. This tether is fabricated and integrated with the rest of the cooler using the following process, shown in Fig. 2(b) and (c).

1) A shallow recess is etched in the top side of a 500-μm-thick silicon wafer using DRIE.
2) A 100-μm-thick Pyrex glass wafer is bonded to the top side of the silicon wafer, covering the recess.
3) A layer of Cr/Au is deposited over the glass and patterned to form a masking layer.
4) The glass wafer is etched in a concentrated HF solution, and the masking metal layer is stripped.
5) The thermal substrate is aligned to the structural substrate, and they are anodically bonded.
6) A shadow mask is aligned to the device wafer and clamped into place. The Bi_2Te_3 film is deposited by coevaporation at a substrate temperature of 260 °C.
7) The shadow mask is switched, and Sb_2Te_3 is deposited at a substrate temperature of 230 °C, completing the coolers. Shadow mask patterning is chosen as the last fabrication step to avoid wet and dry processes which might damage the fragile cooler, be incompatible with the TE deposition temperatures, or contaminate silicon processing tools.

TABLE III
DESIGN PARAMETERS FOR SIMULATED ONE- AND SIX-STAGE COOLERS

TE length	100 μm	
TE width	30 μm	
TE thickness	4 μm	
Contact area	200 μm x 100 μm	
Stage	# of TCs	Size, mm
Stage 1	64	5.0
Stage 2	32	3.5
Stage 3	16	3.0
Stage 4	8	2.5
Stage 5	4	2.0
Stage 6	2	1.5

Fig. 3 shows a six-stage cooler along with a one-stage cooler fabricated through the same process, omitting the glass tether.

IV. MODELING AND DESIGN

To understand multistage coolers and the effect of nonidealities—such as the thermal conduction of the dielectric membrane and contact resistance—on their performance, a 1-D model was developed. One- and six-stage coolers were simulated. The model takes into account all the major TE effects, including Peltier heat transfer, Joule heating from the TE thin films and from contact resistance, and thermal conduction [30]. The model was initially implemented using Matlab and has also been ported to Mathematica. The simulated one-stage cooler and the first stage of the six-stage cooler were identical and measured 5.4 mm on a side, with a total of 64 TCs. The geometry of the TCs, the number of TCs at each stage of the six-stage design, and the size of each of the stages are given in Table III.

The material properties used in the simulations are in Table II. The devices were simulated both with and without the supporting oxide required for the actual device, and in each case, they were simulated once with no contact resistivity (R_c) and once with a high contact resistivity $R_c = 1.24 \times 10^{-8}\ \Omega \cdot \mathrm{m}^2$. This latter value was chosen because it is the resistivity at which the contact resistance of one TC is equal to the intrinsic resistance of the TC. Fig. 4 shows the cooling generated using different input currents, i.e., with different input powers. In the ideal case, with no oxide and no contact resistance, the

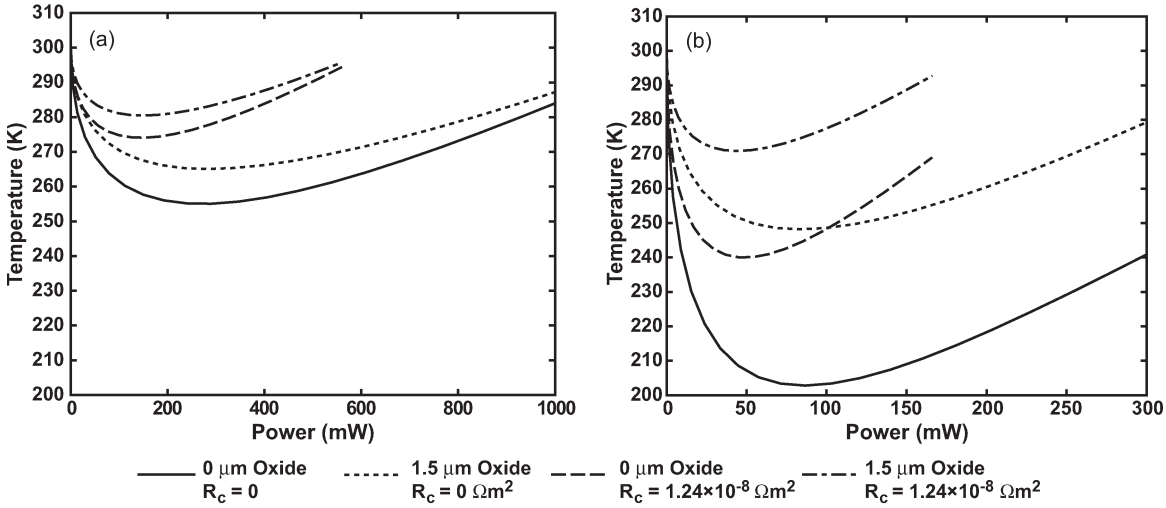

Fig. 4. Predicted thermal performances of (a) a one-stage cooler and (b) a six-stage cooler, with respect to power consumption for two oxide thicknesses and two contact resistivities. Both are shown with and without a 1.5-μm-thick supporting oxide, with contact resistivities of 0 and $1.24 \times 10^{-8}\ \Omega \cdot \mathrm{m}^2$. The latter value, $1.24 \times 10^{-8}\ \Omega \cdot \mathrm{m}^2$, corresponds to the point where the contact resistance is equal to the TE material resistance for one TC.

one-stage cooler is predicted to reach 255.1 K from an ambient temperature of 300 K at a power of more than 200 mW, while the six-stage cooler reaches 202.9 K using less than 100 mW, making the potential benefit of multistage cooling clear.

However, when simulated with the supporting oxide membrane and the elevated contact resistance, the coolers only reach 281.8 K and 272.9 K for the one- and six-stage devices, respectively. In the ideal case, the six-stage cooler achieved a temperature differential more than twice as large as that of the one-stage cooler; however, in the more realistic case, the six-stage cooler was only able to achieve a 49% greater temperature differential, indicating that the effects of contact resistance and the supporting oxide negate some of the benefits of adding multiple stages. To further investigate the parasitic effects of the supporting oxide and contact resistivity, the devices were simulated over a wide range of contact resistivities both with and without the supporting oxide. At each value of contact resistivity, the optimum current and minimum temperature were found. The results are shown in Fig. 5. With a negligible contact resistivity of $1 \times 10^{-11}\ \Omega \cdot \mathrm{m}^2$ and no oxide, the simulated performance of the coolers is the same as that discussed previously in the first case. The effect of contact resistivity is minimal for values less than $1 \times 10^{-9}\ \Omega \cdot \mathrm{m}^2$. Above this, cooler performance rapidly decreases and is significantly degraded at $R_c = 1 \times 10^{-7}\ \Omega \cdot \mathrm{m}^2$. The minimum achievable cold stage temperature slowly approaches 300 K as contact resistance increases further.

A similar trend is seen in the devices simulated with a 1.5-μm-thick layer of oxide to support the TE material (Fig. 5). The results clearly indicate that thermal conduction through the supportive oxide partially negates the benefits of multiple stages. At the lowest contact resistivity, the one- and six-stage coolers reach 265.1 K and 248.2 K. While there is still a performance gain achieved by using multiple stages, the one-stage cooler in this case achieves a temperature differential that is 67% of that achieved by the six-stage cooler. In the ideal case without oxide, the one-stage cooler only achieves

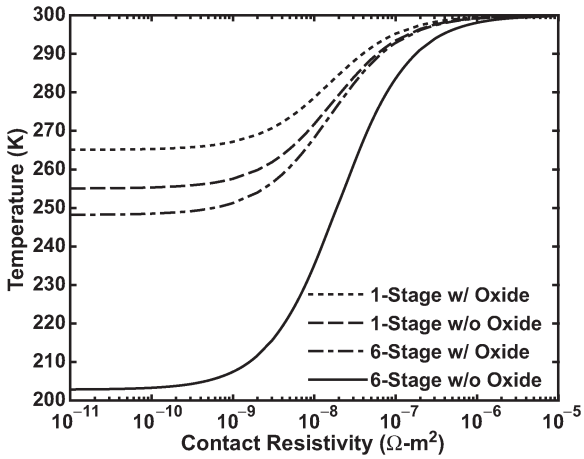

Fig. 5. Variation in thermal performance of one- and six-stage coolers simulated as a function of the contact resistivity. Both cooler designs are simulated under ideal conditions with no oxide supporting the TE material and under realistic conditions with 1.5 μm of oxide. The TE material properties and geometric parameters used in the simulations can be found in Tables II and III.

a temperature differential that is 48% of that of the six-stage design, as noted earlier.

The limited gain of additional stages in nonideal cooler performance is likely due to high relative parasitic losses through the oxide at the highest (coldest) stages. In stages 4, 5, and 6, only a few TE elements cross a dielectric bridge that is effectively several millimeters wide. The total thermal conduction though the dielectric membrane will be several times greater than the thermal conduction through the TE. This leads to a decrease in the effective Z, limiting the benefit from these stages. In contrast, the outer stages have a large number of TCs, so the thermal conduction through the oxide is on the same order of magnitude as or smaller than the conduction through the TE.

Despite the limiting effect of parasitic thermal conduction, a multistage design is still desirable because of its effect on the cooler efficiency per degree of cooling. The six-stage cooler

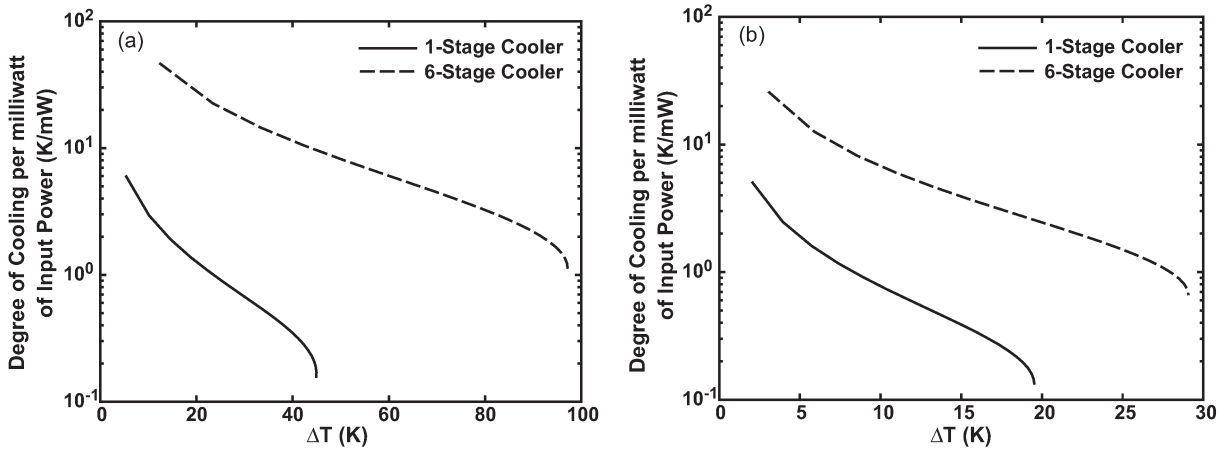

Fig. 6. (a) Predicted degree of cooling per milliwatt as function of cooling for ideal one- and six-stage coolers. (b) Predicted degree of cooling per milliwatt for one- and six-stage coolers, taking into consideration contact resistivity of $1.24 \times 10^{-8}\ \Omega \cdot \mathrm{m}^2$ and a 1.5-μm-thick layer of oxide supporting the TE material.

demonstrates a temperature differential per milliwatt that is at least one order of magnitude greater than that of the one-stage cooler when both are operated at the same temperature differential. This is shown in Fig. 6. Under the ideal assumptions, the one-stage cooler is predicted to use 264 mW at its maximum ΔT of 45 K. At this same ΔT, the six-stage cooler only uses 4.2 mW. Similarly, with the oxide and contact resistivity included, the one-stage cooler would use 148 mW to achieve a temperature difference of 19.5 K, while the six-stage cooler only uses 7.3 mW of power to reach the same result.

V. Testing and Analysis

To experimentally verify these simulation results, two versions of a six-stage cooler plus a one-stage cooler were fabricated and tested. The parameters used to fabricate all three devices are outlined in Table IV, and the devices are shown in Fig. 3. The primary difference between the two 6-stage designs lies in the size and layout of the contact areas and in the perimeters of the stages, which were adjusted to accommodate the modified contact layout. The goal behind the layout of Version 2 was to minimize the overall resistance of the cooler using geometric changes to reduce contact effects. The size of the contact area was increased from $100\ \mu\mathrm{m} \times 100\ \mu\mathrm{m}$ to $100\ \mu\mathrm{m} \times 200\ \mu\mathrm{m}$. In addition, as shown in Fig. 3(c), Version 2 makes use of long segments of TE material that span several stages. This eliminates the need for the current to travel from the TE to the metal and back at every TC in every stage. Finally, by making the silicon somewhat narrower in the stages where this technique is employed, the total resistance of the device can be decreased. The design improvement was confirmed by measurement: The Version-2 cooler has a total series resistance of 816 Ω when operated at its optimal point compared to 977 Ω for the Version-1 cooler, despite the Version-1 cooler having a larger average TE film thickness.

The coolers were tested in a vacuum probe station at a pressure of less than 0.133 Pa (1 mTorr). The temperature was measured using a resistive element in a four-point probe configuration. Fig. 7 shows the results from both versions of the six-stage cooler and the single-stage cooler. Version 1 generated a temperature differential of 16.6 K with an input power 24.4 mW, while Version 2 generated a differential of 22.3 K with an input power of 24.8 mW.

TABLE IV
Design Parameters for Fabricated One- and Six-Stage Coolers

Cooler	TE Length	TE Width	TE thickness (μm)	Contact Area	Oxide Thickness
6-Stage, Version 1	30 μm	100 μm	Sb_2Te_3: 3 .8 Bi_2Te_3: 2.9	100 μm x 100 μm	1.8 μm
6-Stage, Version 2	30 μm	100 μm	Sb_2Te_3: 3 .2 Bi_2Te_3: 2 .7	200 μm x 100 μm	1.5 μm
1-Stage	60 μm	100 μm	Sb_2Te_3: 3 .2 Bi_2Te_3: 2 .7	100 μm x 100 μm	1.5 μm

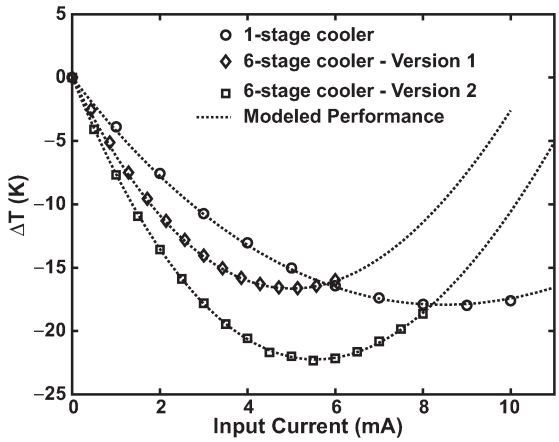

Fig. 7. (Symbols) Measured versus (lines) modeled performance of both versions of the six-stage cooler and the one-stage cooler. Material properties were used as simulation parameters to fit the model to the measured results.

The model described earlier was then fit to the data to estimate the average properties of the *in situ* materials. The Seebeck coefficient, thermal conductivity, and the combined effect of contact resistance and film resistance were used as the fitting parameters. To perform the fit, contact resistance was first fit to a value of $1.03 \times 10^{-8}\ \Omega \cdot \mathrm{m}^2$ to adjust the total resistance of the simulated cooler to the measured resistance of the actual cooler, assuming a resistivity of 20 $\mu\Omega \cdot \mathrm{m}$ for both TE films. This assumption is valid because the important parameter is the total resistance of one TC, which will be correctly accounted for

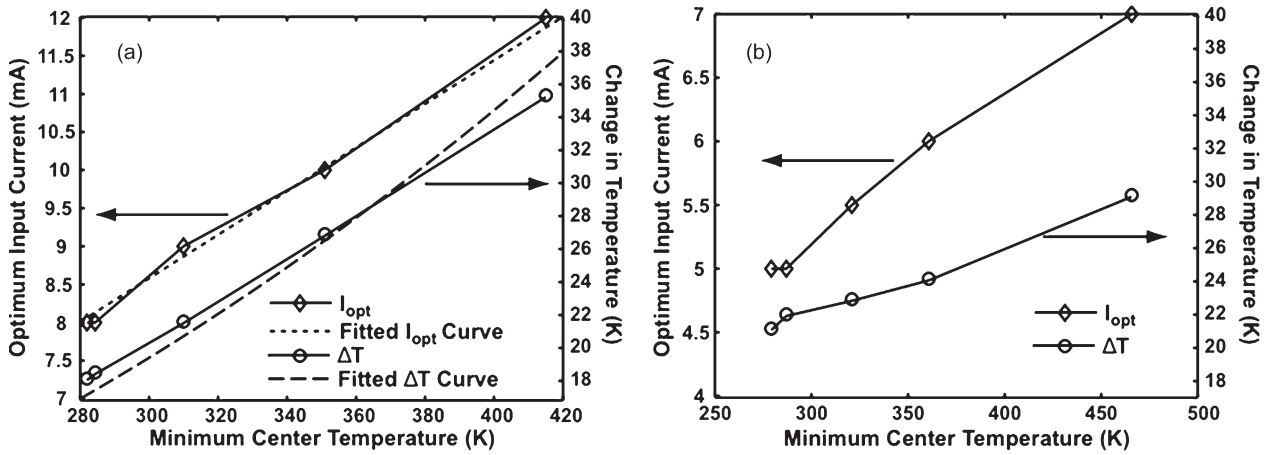

Fig. 8. (Left axes) Optimum input current and (right axes) change in temperature between the OFF and ON states at the center of the cooler under varying thermal load conditions. In all cases, the ambient temperature is maintained at 300 K, and the temperature of the center region is increased by applying a thermal load with a resistive element. (a) Results from a one-stage cooler, along with curves fitted to the physical model. (b) Results from a six-stage cooler.

with the described method. Note that the fitted value of contact resistivity is below the critical value of $1.24 \times 10^{-8}\ \Omega \cdot \mathrm{m}^2$ used in the modeling in Section IV and compares favorably with others' measured values reported in [9], [19], [23], [27], and [31]–[33]. Next, it is assumed that both the p- and n-type materials have the same Seebeck coefficient magnitude, which is adjusted so that the measured optimum current matches the simulated value. Finally, the thermal conductivity of the TE material is adjusted to match the magnitude of the maximum simulated ΔT with the measured results. The model used included the SiO_2 membrane, which was assumed to have a thermal conductivity of $1.15\ \mathrm{W}/(\mathrm{m} \cdot \mathrm{K})$. For Version 1 of the six-stage cooler, the estimated Seebeck coefficient was 180 μV/K, and the estimated thermal conductivity was $1\ \mathrm{W}/(\mathrm{m} \cdot \mathrm{K})$. Version 2 also indicated a thermal conductivity of $1\ \mathrm{W}/(\mathrm{m} \cdot \mathrm{K})$, but its Seebeck coefficient was lower at 166 μV/K. This variation in TE material properties is likely due to inaccurate control of material flux rates and substrate temperature inside the deposition chamber. To understand how the structure of the cooler affected the overall results, the ideal model was fitted to the data and used to calculate an effective Z. In effect, this calculation poses the question: In the absence of parasitic thermal conductance and Joule heating, what figure of merit would produce a six-stage cooler with the measured performance curve? The performance of Version 1 is replicated using a TE material with an effective Z of $1.6 \times 10^{-4}\ \mathrm{K}^{-1}$, corresponding to an effective ZT of 0.048 at 300 K. Version 2 fared slightly better, requiring material with an effective Z of $2.2 \times 10^{-4}\ \mathrm{K}^{-1}$ or an effective ZT of 0.066 at 300 K. However, both effective ZT values are low compared to the intrinsic material properties shown in Table II. This indicates that the TE material is not being effectively utilized in these coolers. As already discussed, this is most likely due to the supportive oxide used in the inner stages.

The one-stage cooler was able to achieve a temperature differential of 17.9 K at a current input of 8.5 mA, as shown in Fig. 7. The effective Z was calculated for the one-stage cooler to be $4.6 \times 10^{-4}\ \mathrm{K}^{-1}$, corresponding to a ZT of 0.13. While significantly closer to the measured intrinsic value, this low number indicates that the performance of the one-stage cooler is also hampered by parasitic effects due to contact resistance and the presence of the oxide membrane. Using the same curve-fitting technique described previously, the average Seebeck coefficient was found to be 185 μV/K, again with an estimated thermal conductivity of $1\ \mathrm{W}/(\mathrm{m} \cdot \mathrm{K})$. This Seebeck coefficient is larger than the value found for the Version-2 six-stage cooler described previously, even though both were fabricated simultaneously on the same wafer. However, it has previously been shown that the Seebeck coefficient of the coevaporated thin films is closely related to the temperature of the substrate during deposition [29]. In the six-stage cooler, the center stages are highly isolated from the substrate, and thus, the temperature of the inner stages may vary from the temperature of the outer stages and the single-stage cooler during deposition. This likely degrades the quality of the material at the inner stages. Parametric analysis of the one-stage cooler was used to estimate the fitting error for material properties: $\pm 2\%$ for the Seebeck coefficient, $\pm 5\%$ for the TE thermal conductivity and TE resistivity, and $\pm 10\%$ for contact resistivity.

Finally, both the one- and six-stage designs were tested under thermal loads. The resistive temperature sensor supplied loads of varying magnitude. As the thermal load was raised, both coolers were able to generate higher differences in temperature between the OFF state and the optimum current (maximum ΔT) point. In addition, both the coolers exhibited an increase in the magnitude of the optimal current. With the cooler off, a 50-mW resistive heating load was applied, raising the center of the one-stage device to 450.3 K. When a current was applied, I_{opt} was found to have increased to 12 mA, and the center region was cooled to 415.0 K. This represents a change of 35.3 K, compared to only 18.0 K using an 8-mA current when the device was loaded with 100 μW. Similarly, with a 25-mW load, the six-stage device was able to reduce the temperature of the cooler region from 494.9 K to 465.8 K, a change of 29.1 K with an optimum current of 7 mA. This apparent improvement in performance is a result of the temperature dependence of ΔT_{max}, as described by (1). Fig. 8 shows this effect for both the one- and six-stage coolers. The data from the one-stage cooler

are shown in Fig. 8(a) along with curves fitted to the ideal cooling equations. The change in temperature of the center stage is fit to (1) and results in a calculated $Z = 4.3 \times 10^{-4} \pm 2.6 \times 10^{-5}$ K^{-1} with a 95% confidence interval. This corresponds to ZT of 0.13 $\pm$ 0.007, which is identical to the ZT value calculated previously for the one-stage cooler. The relationship between temperature and the optimum current was fit to (4) and produced $\alpha_S/R_e = 2.87 \times 10^{-5} \pm 5 \times 10^{-7}$ $\mathrm{A \cdot K^{-1}}$, which fits the data with a sum-of-square error of 5.56×10^{-8}. The excellent fit suggests that the one-stage cooler obeys the ideal equations (1)–(5). The data for the six-stage cooler are shown in Fig. 8(b). However, because the six-stage cooler is more complex, the aforementioned equations are too simplistic to model the relationship between ΔT and I_{opt} and T_{center}, and it is therefore difficult to extract a value of effective Z from these data.

Lower thermal loads were used to measure the thermal resistance of the total structure. The one-stage cooler increased its temperature by 2.7 K upon application of a 1-mW load, leading to a calculated thermal resistance of 2700 K/W. This implies that ΔT would be equal to zero when a 6.6-mW load is applied. The one-stage cooler consumes 14.6 mW under maximum cooling when a 10-mW load is supplied. Therefore, the estimated coefficient of performance (COP) of the cooler (the cooling capacity divided by the power consumption) at $\Delta T = 0$ is 0.45. The temperature of the center stage of a Version-2 six-stage cooler tested under a 1-mW thermal load increased by 8.9 K from a base temperature of 279.2 K. It uses 20.8 mW of power for maximum cooling under a 10-mW load. This corresponds to a thermal resistance of 8900 K/W and a 2.3-mW load to achieve $\Delta T = 0$. The approximate COP at $\Delta T = 0$ is 0.1.

VI. Conclusion

This paper has demonstrated the feasibility of low-power TE microcoolers and has demonstrated the first six-stage planar TE microcooler. Cooling of 22.3 K relative to ambient has been achieved with less than 25 mW of power input. While this is not yet competitive with current commercial options in terms of temperature differential, it uses an order of magnitude less power per degree of cooling. Additionally, the investigation of simulated coolers shows that there is a clear path to achieving higher temperature differences and to realizing a higher degree of differentiation between the one- and six-stage microcoolers. This path includes reducing the parasitic resistance of the cooler, particularly at the contacts, and removing as much of the parasitic thermal conduction paths as possible, particularly at the innermost stages.

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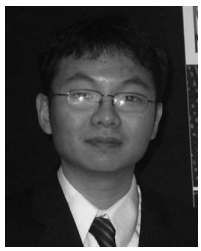

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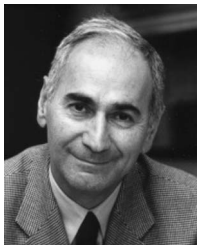

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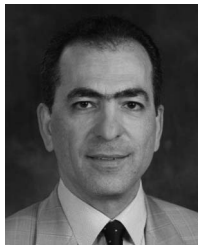

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