

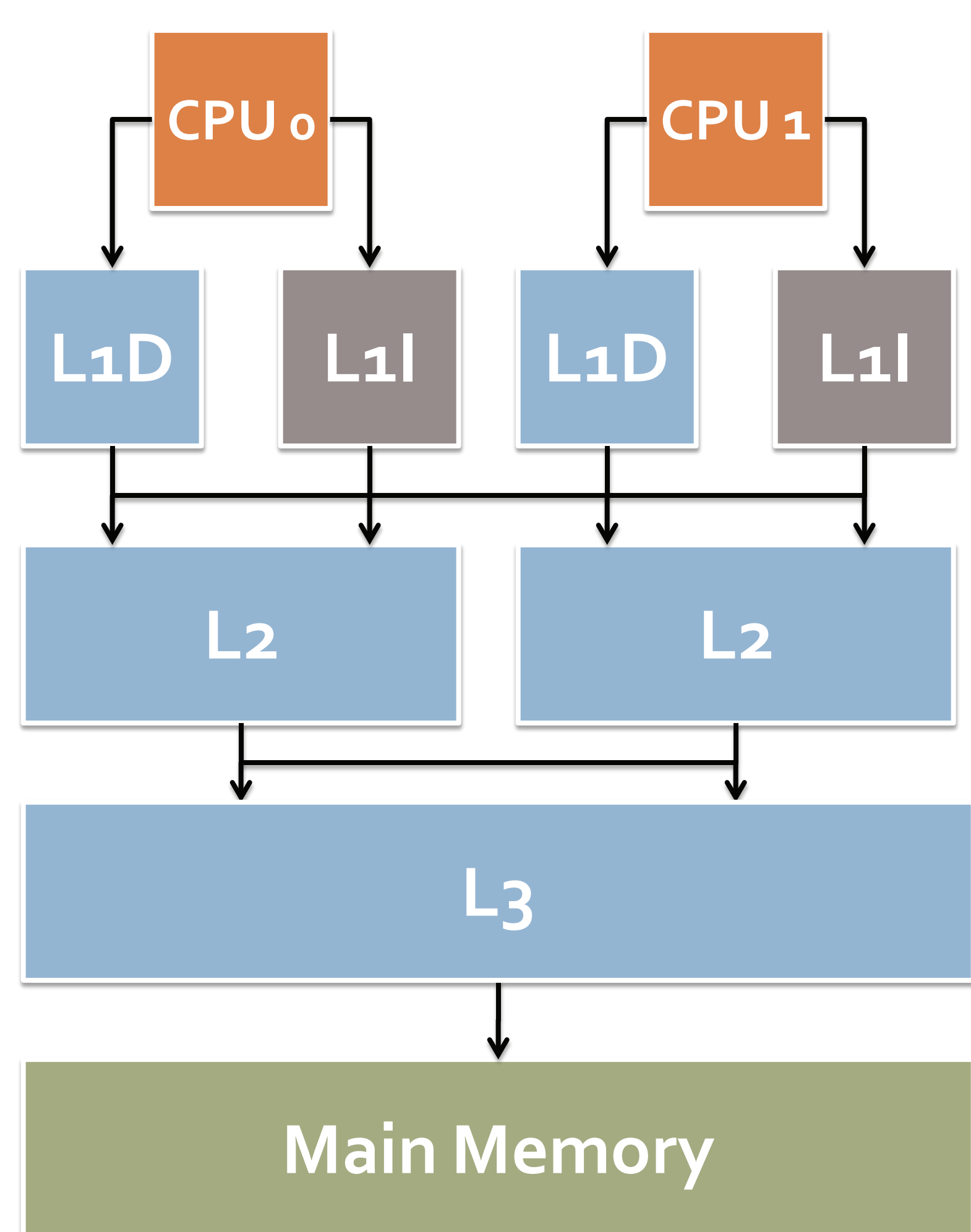
Speculative Cache Coherence

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Cache on Multicore

Maintaining consistency of shared data stored in multiple caches is hard.



Problems:

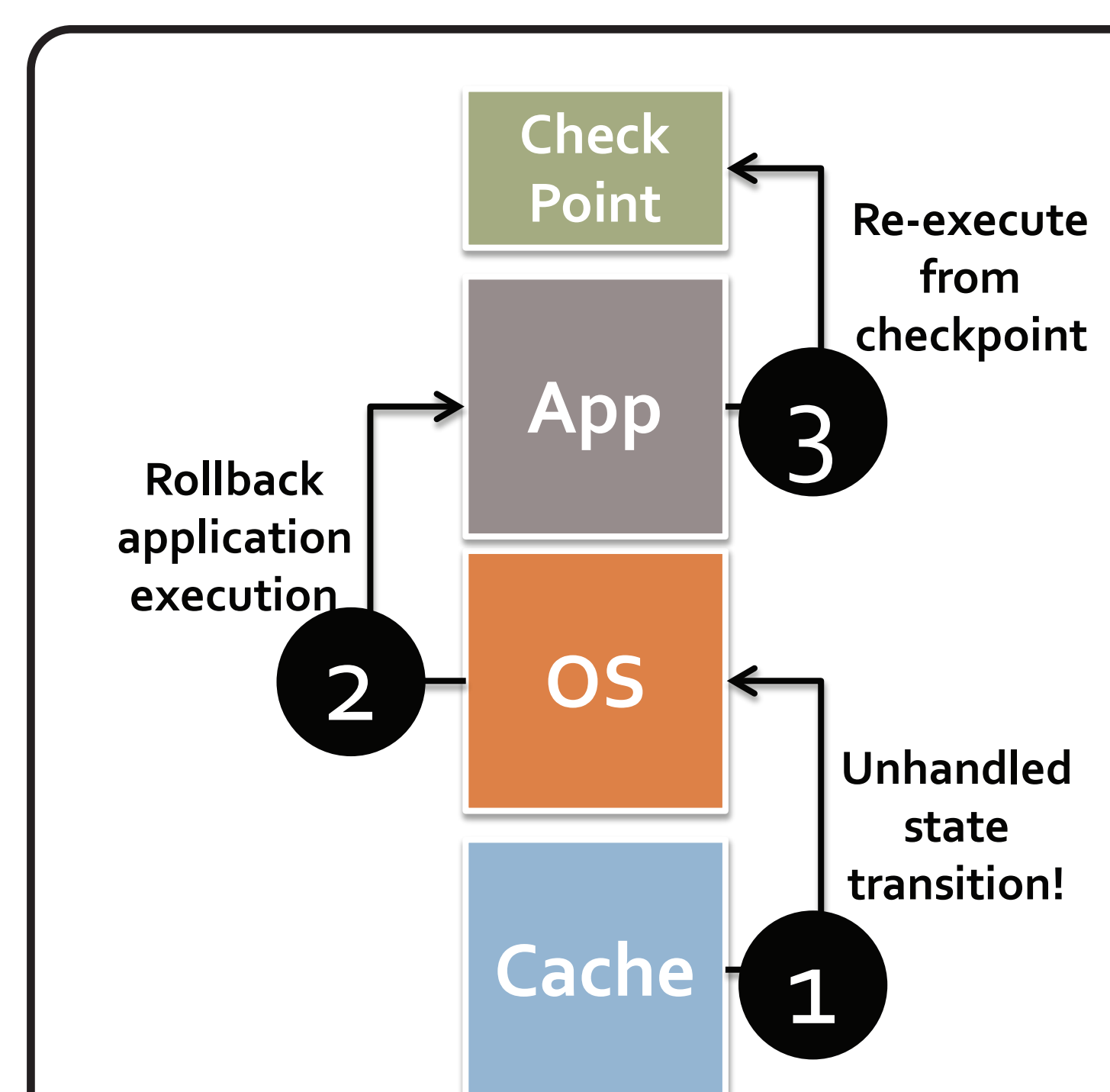
- Hard to provide cache consistency
- Difficult to design, verify cache coherence protocols

Solution:

- Implement common case in *hardware*
- Guarantee consistency in *software*

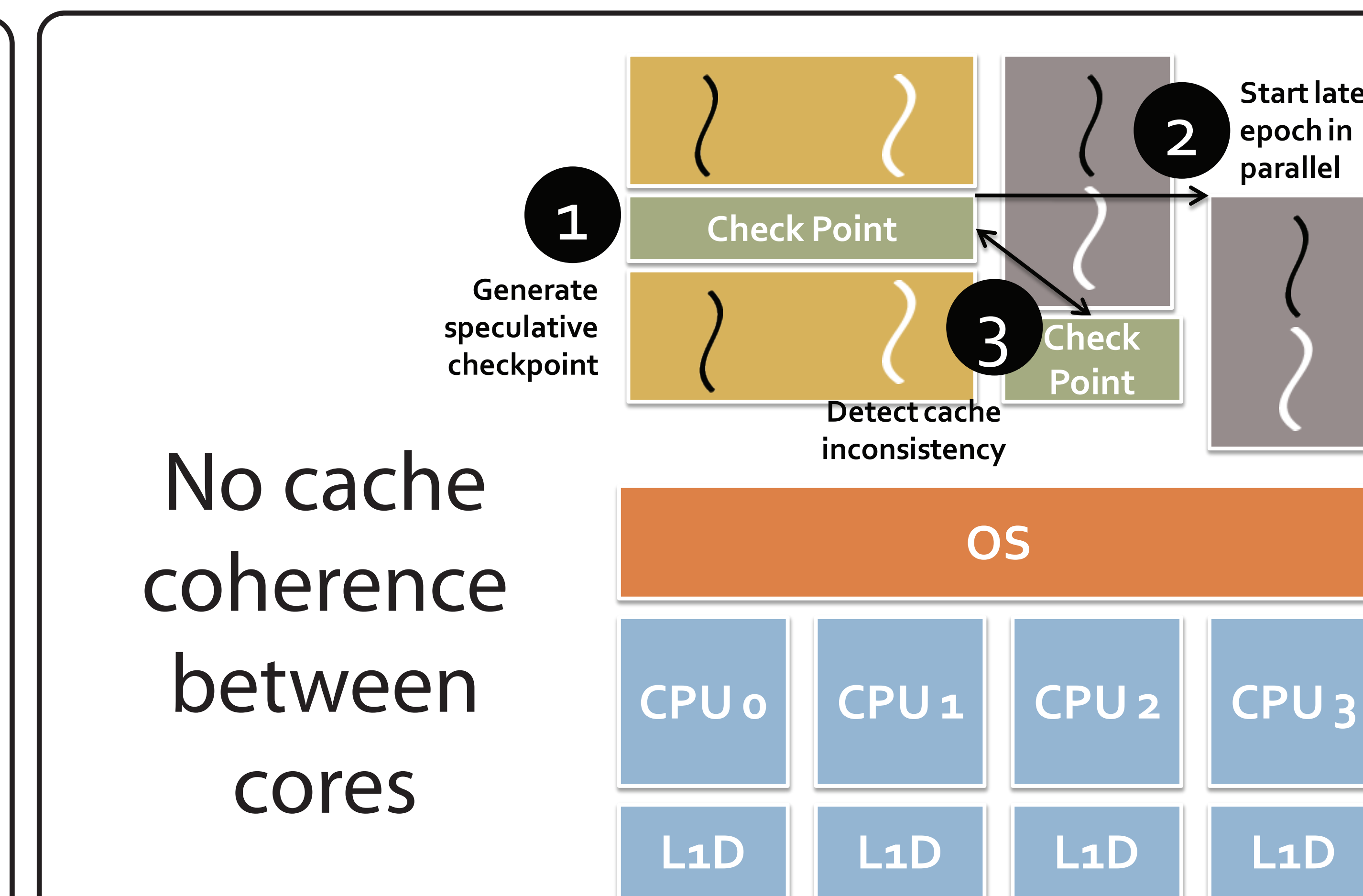
Speculative Cache Coherence

Simplify hardware & improve scalability



Hardware does not support rare state transitions

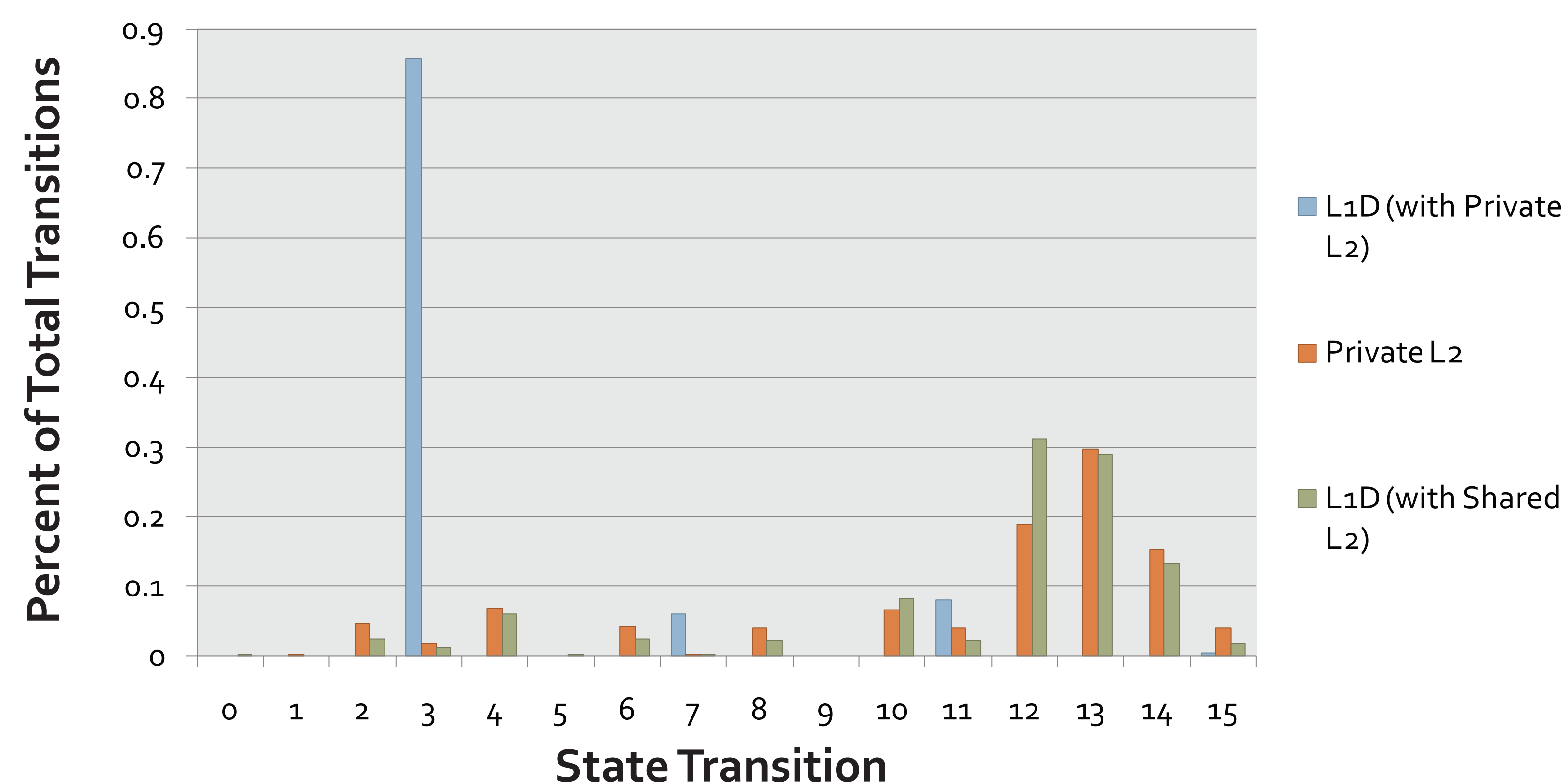
Detect and Re-Execute



No cache coherence between cores

Uniparallel Execution

MESI Cache Coherence Protocol Behavior



Few transitions execute frequently

- Hardware complexity dominated by rare corner cases
- Infrequent state transitions can be handled by software

		MESI State Transitions			
		Initial State			
Final State	M	0	1	2	3
	E	4	5	6	7
	S	8	9	10	11
	I	12	13	14	15