CLASS #7: INTRODUCTION TO OP-AMPS

DORF: CH 6.1-6.5

OBJ: 1) INTRODUCE OP-AMP AND ITS PRINCIPLES
      2) DEFINE IDEAL OPERATIONS
      3) CONDUCT SIMPLE DESIGN OF OP-AMP CIRCUITS

1) OP-AMP
- SHORT FOR OPERATIONAL AMPLIFIER
- MADE FROM TRANSISTORS
- TRUE AMPLIFIER

\[ V_o = A(V_2 - V_1) \]

\[ V_1 \]
\[ V_2 \]
\[ V_o \]

INV INPUT \( V_1 \)

INPUT \( V_2 \)

OUTPUT \( V_o \)

- INFINITE RESISTANCE \( R = \infty \)

i) \( V_1 = V_2 = 0 \)

ii) \( V_2 = V_1 \)

2 KEY PRINCIPLES

NON-Ideal

\[ V_o = A_o(V_2 - V_1) \]

A_o \( \sim 10^4 \) to \( 10^6 \)

\( R_{in} \) \( \sim 10^6 \) to \( 10^{12} \) \( \Omega \)

\( R_{out} \) \( \sim 10^4 \) to \( 10^6 \) \( \Omega \)
3) \textbf{LINEARITY}

i) \(|V_o| \leq V_{\text{sat}}\)

ii) \(|i_o| \leq i_{\text{sat}}\)

iii) \(|\frac{dV_o}{dt}| \leq \text{ slew rate}\)
Common-mode rejection ratio (CMRR). The input to a difference amplifier, in general, contains two components: a common-mode and a difference-mode signal. The common-mode signal voltage is the average of the two inputs, whereas the difference-mode signal is the difference between the two inputs. Ideally, an amplifier affects the difference-mode signals only. However, the common-mode signal is also amplified to some degree. The common-mode rejection ratio (CMRR), which is defined as the ratio of the difference signal voltage gain to the common-mode signal voltage gain provides an indication of how well an op amp does at rejecting a signal applied simultaneously to both inputs. The greater the value of the CMRR, the better is the performance of the op amp.

\[
\text{CMRR} = \frac{\text{Gain (on diff.-mode)}}{\text{Gain (on common-mode)}} \quad \text{A} \uparrow \quad \text{A} \to 0
\]

### TABLE 7.1 Sample Op Amp Specifications

<table>
<thead>
<tr>
<th>Type</th>
<th>Total Supply Voltage</th>
<th>Offset Voltage</th>
<th>Current</th>
<th>Slew Rate</th>
<th>Output Current</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MAX (V)</td>
<td>MIN (V)</td>
<td>MAX (mV)</td>
<td>TYPICAL (mV)</td>
<td>MAX (mA)</td>
</tr>
<tr>
<td>Bipolar</td>
<td>741C</td>
<td>10</td>
<td>36</td>
<td>2.8</td>
<td>2</td>
</tr>
<tr>
<td>MOSFET</td>
<td>CA3420A</td>
<td>2</td>
<td>22</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>JFET</td>
<td>LF411</td>
<td>10</td>
<td>36</td>
<td>3.4</td>
<td>0.8</td>
</tr>
<tr>
<td>Bipolar,</td>
<td>precision</td>
<td>1</td>
<td>45</td>
<td>0.4</td>
<td>0.3</td>
</tr>
</tbody>
</table>

Source: Practical Electronics for Inventors

By Sherz
Differential-input voltage range. Range of voltage that may be applied between input terminals without forcing the op amp to operate outside its specifications. If the inputs go beyond this range, the gain of the op amp may change drastically.

Differential input impedance. Impedance measured between the noninverting and inverting input terminals.

Input offset voltage. In theory, the output voltage of an op amp should be zero when both inputs are zero. In reality, however, a slight circuit imbalance within the internal circuitry can result in an output voltage. The input offset voltage is the amount of voltage that must be applied to one of the inputs to zero the output.

Input bias current. Theoretically, an op amp should have an infinite input impedance and therefore no input current. In reality, however, small currents, typically within the nanoamp to picoamp range, may be drawn by the inputs. The average of the two input currents is referred to as the input bias current. This current can result in a voltage drop across resistors in the feedback network, the bias network, or source impedance, which in turn can lead to error in the output voltage. Input bias currents depend on the input circuitry of an op amp. With FET op amps, input bias currents are usually small enough not to cause serious offset voltages. Bipolar op amps, on the other hand, may cause problems. With bipolar op amps, a compensation resistor is often required to center the output. I will discuss how this is done in a minute.

Input offset current. This represents the difference in the input currents into the two input terminals when the output is zero. What does this mean? Well, the input terminals of a real op amp tend to draw in different amounts of leakage current, even when the same voltage is applied to them. This occurs because there is always a slight difference in resistance within the input circuitry for the two terminals that originates during the manufacturing process. Therefore, if an op amp’s two terminals are both connected to the same input voltage, different amounts of input current will result, causing the output to be offset. Op amps typically come with offset terminals that can be wired to a potentiometer to correct the offset current. I will discuss how this is done in a minute.

Voltage gain ($A_V$). A typical op amp has a voltage gain of $10^4$ to $10^6$ (or 80 to 120 dB; 1 dB = $20 \log_{10} A_V$) at dc. However, the gain drops to 1 at a frequency called the unity-gain frequency $f_u$, typically from 1 to 10 MHz—a result of high-frequency limitations in the op amp’s internal circuitry. I will talk more about high-frequency behavior in op amps in a minute.

Output voltage swing. This is the peak output voltage swing, referenced to zero, that can be obtained without clipping.

Slew rate. This represents the maximum rate of change of an op amp’s output voltage with time. The limitation of output change with time results from internal or external frequency compensation capacitors slowing things down, which in turn results in delayed output changes with input changes (propagation delay). At high frequencies, the magnitude of an op amp’s slew rate becomes more critical. A general-purpose op amp like the 741 has a 0.5 V/μs slew rate—a relatively small value when compared with the high-speed HA2539’s slew rate of 600 V/μs.

Supply current. This represents the current that is required from the power supply to operate the op amp with no load present and with an output voltage of zero.

Table 7.1 is a sample op amp specifications table.