REAL WORLD SIGNALS

In general, signals from sensors do not have suitable characteristics for display/analysis:

- Low amplitude → Amplify (today)
- Noise → Filter (later)

OPERATIONAL-AMP BASICS

For the purposes of this class, we'll be dealing with the "ideal" op-amp model:

\[ V_o = A(V_+ - V_-) \]

which refers to this basic model:

\[ V_o \]
\[ V_+ \]
\[ V_- \]
\[ V_{cc} \]
\[ V_{ee} \]
\[ V_o = (V_+ - V_-) \cdot A \]

We can see that the op-amp "saturates" at two points:

SATURATION

\[
\begin{align*}
\text{FOR } (V_+ - V_-) \cdot A &> V_{cc} \Rightarrow V_o = V_{cc} \\
\text{FOR } (V_+ - V_-) \cdot A &< V_{ee} \Rightarrow V_o = V_{ee} \\
\text{ELSE } &V_o = (V_+ - V_-) \cdot A
\end{align*}
\]
For example: Common OP-AMP

\[ A = 200,000 \quad V_{EE} = 10\text{V} \quad V_{CC} = -10\text{V} \]

- Then saturation would occur at \( \pm 50\text{mV} \)!
- That's not much of an input range
- It's obvious that we want a bit more control over our signal

**Shifting the Range**

- If we know the expected range of our input signal \( V_i \), then we can select \( V_0 \) to shift the linear range

![Diagram of OP-AMP with V_in, V_ref, V_out, V_0, and V_CE labels]

**Changing the Gain (A)**

- We can change the gain by feeding the output \( V_0 \) back into the OP AMP

**Non-inverting Amplifiers**

Find \( V_0 \) for the following circuit

![Diagram of non-inverting amplifier]

\[ V_0 = A(V_i - V_-) \]

Then for large \( A \to \infty \)

\[ \frac{V_0}{A} \approx 0 = V_i - V_- \quad \Rightarrow \quad V_i = V_- \]
From our basic voltage divider

\[ V_- = \frac{R_i}{R_2 + R_i} \quad V_o = V_+ \quad (\text{so since } V_- = V_+) \]

Then

\[ V_o = \frac{V_i}{\frac{R_1}{R_2 + R_1}} = V_i \left(1 + \frac{R_2}{R_1}\right) \]

---

New gain depends only on \( V_i \)

---

...called a non-inverting amp B.C. the voltage changes in same direction as input
MEASURING ANALOG SIGNALS

- Computers can only perform operations on digital or discrete values

![Graph showing original and digitized signal](image)

**DEF:** An **analog to digital converter (ADC) (A/D)** is an electronic circuit that transforms an analog signal to a discrete form.

**Resolution:** The smallest change in an analog signal that will result in a discrete output

Resolution: \[ \Delta V = \frac{V_{\text{rep}}}{2^n} \] voltage range

\[ 2^n \] total # of discrete values

Where \( n \) is the number of bits of the digital output.
EXAMPLE: A 4-BIT ADC with a 0-4V RANGE will give \( 2^4 = 16 \) DISCRETE VALUES with \( \Delta V = 0.25V \)

- THE RESOLUTION \( \Delta V \) REPRESENTS THE QUANTIZATION ERROR INHERENT IN THE CONVERSION

- COMMON VALUES FOR N ARE: 2, 4, 8, 10, 12, 20, 24 BIT

- TO IMPROVE THE ACCURACY OF OUR ADC WE CAN:
  1. INCREASE THE RESOLUTION (MORE BITS) IMPROVE MEASUREMENT OF SIGNAL AMPLITUDE
  2. INCREASE SAMPLING RATE (CLOCK SPEED) IMPROVE TEMPORAL RESOLUTION

\[ \text{SIGNAL} \xrightarrow{\text{ADC}} \text{M} \]

\[ \text{M} \xrightarrow{\text{CLOCK SPEED}} \]
BUILDING ADCS

RECALL THAT OP-AMPS HAVE A VERY NARROW LINEAR RANGE:

![Graph showing the linear range of an op-amp](image)

LOOKS MORE LIKE THIS

![Graph showing a narrow jump](image)

WE CAN EXPLOIT THIS VERY NARROW LINEAR RANGE TO BUILD A VOLTAGE COMPARATOR

EXAMPLE: SAY THAT WE WANT TO LABEL A SIGNAL AS EITHER BEING SMALLER OR LARGER THAN .3V WITH A MARGIN OF ERROR OF .05V

![Diagram showing voltage comparator](image)
Since our linear region is so small (UV) compared to our expected threshold of 0.5V then

\[ V_o = 0V \text{ (GND)} \text{ for } V_{in} < 3V \]
\[ V_o = 5V \text{ for } V_{in} > 3V \]

This voltage comparator gives us a "binary" response (1 bit ADC!)

We can now stack a bunch of these together to get more complex ADC architectures
THE FLASH ADC

Each op amp will trigger at a different value.

The above example allows us to determine 4 unique values of $V_{IN}$.

Then $4 = 2^n \Rightarrow n = 2 \Rightarrow 2$-bit ADC

In general, it can be shown that for the generic flash $n$-bit ADC we need $2^n - 1$ comparators and $2^n$ resistors.
**Flash ADC**

**Pro**
- Simple
- Fast
- Almost instantaneous

**Con**
- Many components/parts
- Expensive

---

New component: Digital to Analog Converter (DAC)

- Takes an input voltage $V_{\text{ref}}$ and a command from a controller (computer)
- Outputs a voltage $V_o$ at a resolution of $n$-bits

\[
\begin{array}{c}
V_{\text{ref}} \\
\downarrow \\
\text{DAC} \\
\downarrow \\
\text{Command} \\
\downarrow \\
V_o \\
\uparrow \\
3 \Delta V_{\text{ref}} \\
\end{array}
\]

- A DAC is essentially the opposite of an ADC
- A simple DAC can be made by reversing our Flash ADC (see HW)
The Successive Approximation (SAR) ADC

- Uses DAC to make ADC

How it works

- Initial guess: The controller tells the n-bit DAC to generate an output value
- The output of the DAC is then compared to $V_{\text{in}}$
- The output of the comparator tells us if the guess is too "high" or too "low"
- The controller then adjusts the output of the DAC to guess again
- This repeats until we find $V_{\text{in}}$
**PROS**

- Lower cost (NOT CHEAP) though
- Can be easily built for high res.

**CON**

- Slower speed at high accuracies due to the need to compare many values
NEW COMPONENT: THE INTEGRATOR

DERIVE \( V_o \) FOR THE FOLLOWING

\[
\begin{align*}
\text{RECALL:} & \quad i_c = C \frac{dV_c}{dt} \\
& \quad V_n = \frac{-i_c}{C} \\
& \quad i_n = i_c \quad \text{(SEE INVERTING AMPLIFIER Ex.)} \\
& \quad \text{THEN} \\
& \quad i_n = -i_c \\
& \quad \frac{V_{in}}{R} = -C \frac{dV_o}{dt} \quad \Rightarrow \quad \frac{dV_o}{dt} = -\frac{V_{in}}{RC} \\
& \quad \text{ASSUME} \ V_o = 0 \ \text{INITIALLY AND INTEGRATE:} \\
& \quad \int_0^t \frac{dV_o}{dt} \, dt = -\frac{1}{RC} \int_0^t V_{in} \, dt \\
& \quad V_o = -\frac{1}{RC} \int_0^t V_{in} \, dt
\end{align*}
\]

SCHEMATIC

\[
\begin{align*}
V_{in} & \rightarrow \quad \text{Operational Amplifier} \\
\end{align*}
\]
THE DUAL SCUPE ADC

- Using the integrator, we can make an ADC

![Circuit Diagram]

**How It Works:**

1. Flip switch S to VIN position for a fixed duration: TINT  
   \[ V_{INT} \text{ increases} \]

2. Then flip switch S to -VREF  
   \[ V_{INT} \text{ decreases} \]

Hold S on -VREF until comparator detects that the output of the integrator is zero

\[ V_{IN} = \frac{V_{REF}}{T_{DE-INT}} \cdot T_{INT} \]
Measure the time it takes the comparator to detect that \( V_{\text{int}} \) has crossed \( \pm E_{\text{OL}} \), and calc \( V_{\text{in}} \)

**Dual Slope ADC**

**Pros**
- Can go to high res
- (15+ bits)

**Cons**
- Slow
- Relies on quality components
**Delta Sigma ADC**

- Based on quantizing difference between samples, rather than abs. value

**Based on Delta Modulator:**

- From the analog signal an estimate \( \hat{x}(t) \) is integrated and subtracted away from \( x(t) \) to calc. error \( \varepsilon(t) \)

\[
\varepsilon(t) = x(t) - \hat{x}(t)
\]

- The error is then fed to a 1-bit comparator (quantizer)

\[
Y(t) = V_{\text{REF}} \quad \text{when} \quad \varepsilon(t) > 0
\]

\[
Y(t) = -V_{\text{REF}} \quad \text{when} \quad \varepsilon(t) < 0
\]
This essentially "tracks" the input signal.

\[ -x(t) \]

\[ -x(t+1) \]

\[ V_{rep} \]

\[ V_{rep} \]

Accuracy then depends on \( V_{rep} \) and sampling time \( \Delta t \).
Due to linearity, we can move the integrator to the front to get the **Sigma Delta ADC** (or ΔΣ-ADC).

\[ x(t) \xrightarrow{\Sigma} y(t) \]

If we oversample the signal \( x(t) \), the average output \( y(t) \) will be proportional to \( x(t) \).

**Example:** If we want to sample \( x(t) \) at a rate of 1/sec, the ΔΣ-ADC would sample at 100+ samples/sec.

**Pros:**
- Super-high res.
- Almost all digital

**Cons:**
- Slow due to oversampling